SONY

Diagonal 6.23 mm (Type 1/2.9) CMOS Image Sensor with Square Pixel for Color Cameras

Preliminary

IMX323LQN-C

Description

The IMX323LQN-C is a diagonal 6.23 mm (Type 1/2.9) CMOS active pixel type image sensor with a square pixel array and approximately 2.12 M active pixels. This chip operates with analog 2.7 V, digital 1.2 V, and interface 1.8 V triple power supplies. High sensitivity, low dark current and no smear are achieved through the adoption of R, G and B primary color pigment mosaic filters. This chip features an electronic shutter with variable integration time.
(Applications: Consumer use drive recorder, Consumer use network camera)

Features

- ◆CMOS active pixel type dots
- ◆Input clock frequency: 37.125 MHz
- ◆Readout mode
  HD1080 p mode
  HD720 p mode
- ◆Variable-speed shutter function (Minimum unit: One horizontal sync signal period (1XHS))
- ◆H driver, V driver and serial communication circuit on chip
- ◆DCK sync mode supported
- ◆CDS/PGA on chip
  0 dB to 21 dB: Analog Gain 21 dB (step pitch 0.3 dB)
  21.3 dB to 45 dB: Analog Gain 21 dB + Digital Gain 0.3 to 24 dB (step pitch 0.3 dB)
- ◆10-bit / 12-bit A/D converter on-chip
- ◆CMOS logic parallel SDR Data-Clock output
- ◆R, G, B primary color pigment mosaic filters on chip
- ◆Recommended lens F value: 2.8 or more (close side)
- ◆Recommended exit pupil distance: –30 mm to –∞

Exmor

Sony reserves the right to change products and specifications without prior notice.
This information does not convey any license by any implication or otherwise under any patents or other right.
Application circuits shown, if any, are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits.

Rev.0.2

Device Structure

- CMOS image sensor
- Image size
  Diagonal 6.23 mm (Type 1/2.9)
- Total number of pixels
  2001 (H) × 1121 (V) approx. 2.24 M pixels
- Number of effective pixels
  1985 (H) × 1105 (V) approx. 2.19 M pixels
- Number of active pixels
  1936 (H) × 1097 (V) approx. 2.12 M pixels
- Number of recommended recording pixels
  1920 (H) × 1080 (V) approx. 2.07 M pixels
- Unit cell size
  2.8 µm (H) × 2.8 µm (V)
- Optical black
  Horizontal (H) direction: Front 16 pixels, rear 0 pixels
  Vertical (V) direction: Front 16 pixels, rear 0 pixels
- Dummy
  Horizontal (H) direction: Front 0 pixels, rear 0 pixels
  Vertical (V) direction: Front 7 pixels, rear 0 pixels
- Substrate material
  Silicon

Absolute Maximum Ratings

Supply voltage (analog 2.7 V)	AV_{DD}	–0.3 to +3.3	V
Supply voltage (digital 1.2 V)	DV_{DD}	–0.3 to +2.0	V
Supply voltage (digital 1.8 V)	OV_{DD}	–0.3 to +3.3	V
Input voltage (digital)	V_I	–0.3 to OV_{DD} +0.3	V
Output voltage (digital)	V_O	–0.3 to OV_{DD} +0.3	V
Guaranteed Operating temperature	Topr	–30 to +75	˚C
Guaranteed storage temperature	Tstg	–40 to +80	˚C
Guaranteed performance temperature	Tspc	–10 to +60	˚C

Recommended Operating Conditions

Supply voltage (analog 2.7 V)	AV_{DD}	2.7 ± 0.1	V
Supply voltage (digital 1.2 V)	DV_{DD}	1.2 ± 0.1	V
Supply voltage (digital 1.8 V)	OV_{DD}	1.8 ± 0.1	V
Input voltage (digital)	V_I	–0.1 to OV_{DD}+0.1	V
Output voltage (digital)	V_O	–0.1 to OV_{DD}+0.1	V

USE RESTRICTION NOTICE

This USE RESTRICTION NOTICE ("Notice") is for customers who are considering or currently using the image sensor products ("Products") set forth in this specifications book. Sony Corporation ("Sony") may, at any time, modify this Notice which will be available to you in the latest specifications book for the Products. You should abide by the latest version of this Notice. If a Sony subsidiary or distributor has its own use restriction notice on the Products, such a use restriction notice will additionally apply between you and the subsidiary or distributor. You should consult a sales representative of the subsidiary or distributor of Sony on such a use restriction notice when you consider using the Products.

Use Restrictions

- The Products are intended for incorporation into such general electronic equipment as office products, communication products, measurement products, and home electronics products in accordance with the terms and conditions set forth in this specifications book and otherwise notified by Sony from time to time.
- You should not use the Products for critical applications which may pose a life- or injury-threatening risk or are highly likely to cause significant property damage in the event of failure of the Products. You should consult your sales representative beforehand when you consider using the Products for such critical applications. In addition, you should not use the Products in weapon or military equipment.
- Sony disclaims and does not assume any liability and damages arising out of misuse, improper use, modification, use of the Products for the above-mentioned critical applications, weapon and military equipment, or any deviation from the requirements set forth in this specifications book.

Design for Safety

- Sony is making continuous efforts to further improve the quality and reliability of the Products; however, failure of a certain percentage of the Products is inevitable. Therefore, you should take sufficient care to ensure the safe design of your products such as component redundancy, anti-conflagration features, and features to prevent mis-operation in order to avoid accidents resulting in injury or death, fire or other social damage as a result of such failure.

Export Control

- If the Products are controlled items under the export control laws or regulations of various countries, approval may be required for the export of the Products under the said laws or regulations. You should be responsible for compliance with the said laws or regulations.

No License Implied

- The technical information shown in this specifications book is for your reference purposes only. The availability of this specifications book shall not be construed as giving any indication that Sony and its licensors will license any intellectual property rights in such information by any implication or otherwise. Sony will not assume responsibility for any problems in connection with your use of such information or for any infringement of third-party rights due to the same. It is therefore your sole legal and financial responsibility to resolve any such problems and infringement.

Governing Law

- This Notice shall be governed by and construed in accordance with the laws of Japan, without reference to principles of conflict of laws or choice of laws. All controversies and disputes arising out of or relating to this Notice shall be submitted to the exclusive jurisdiction of the Tokyo District Court in Japan as the court of first instance.

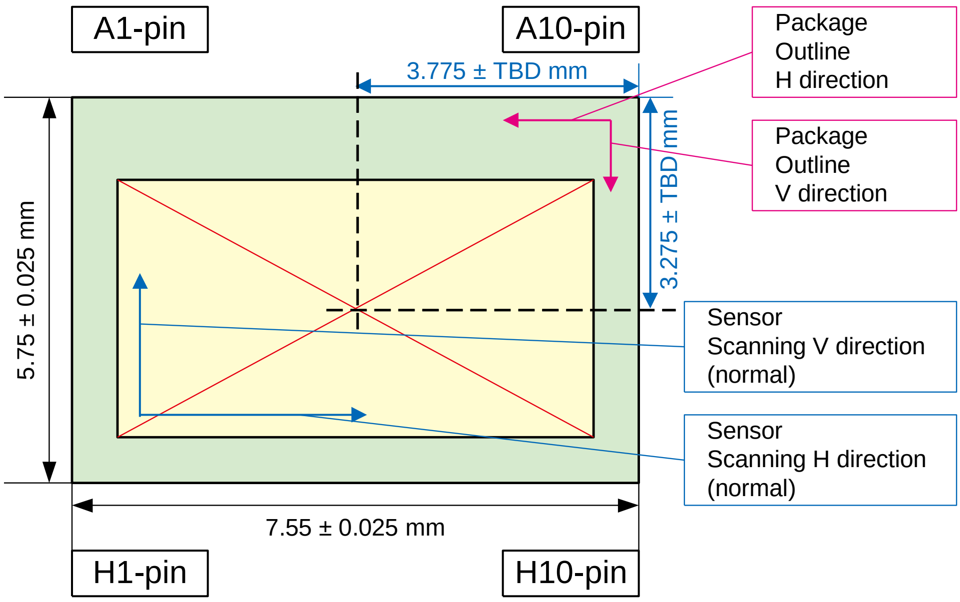
Other Applicable Terms and Conditions

- The terms and conditions in the Sony additional specifications, which will be made available to you when you order the Products, shall also be applicable to your use of the Products as well as to this specifications book. You should review those terms and conditions when you consider purchasing and/or using the Products.

General-0.0.8

CONTENTS

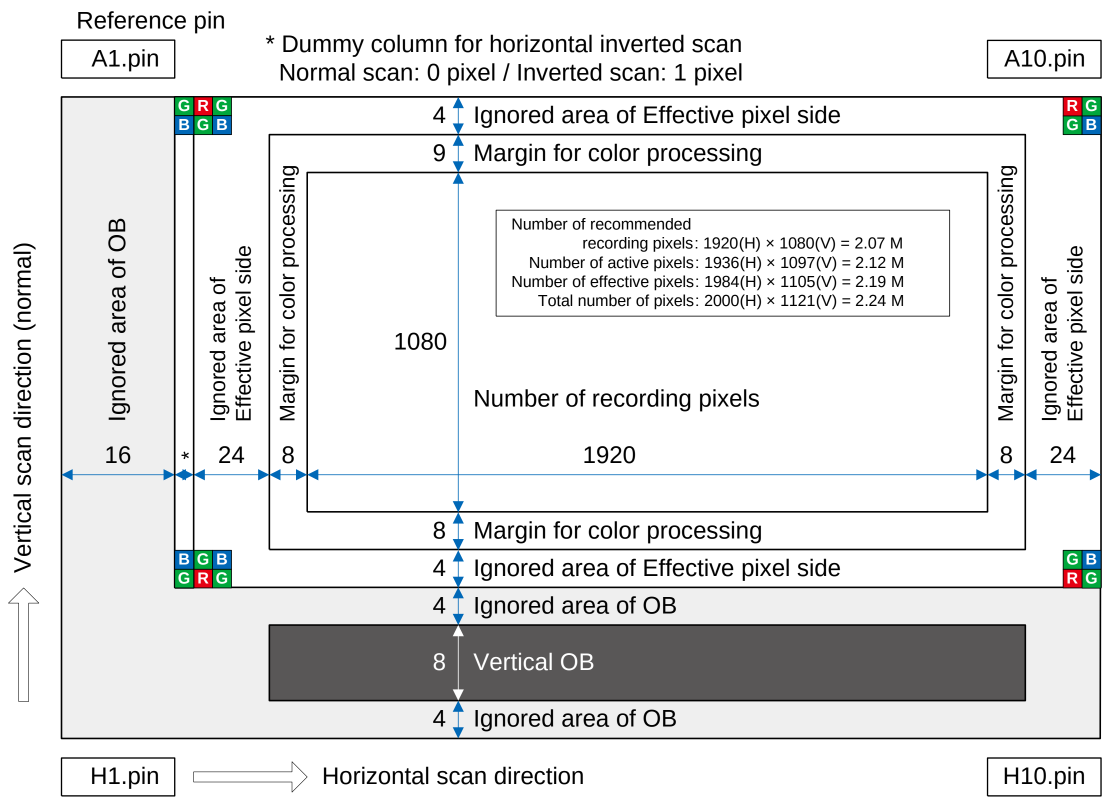
Chip Center and Optical Center



Optical Center

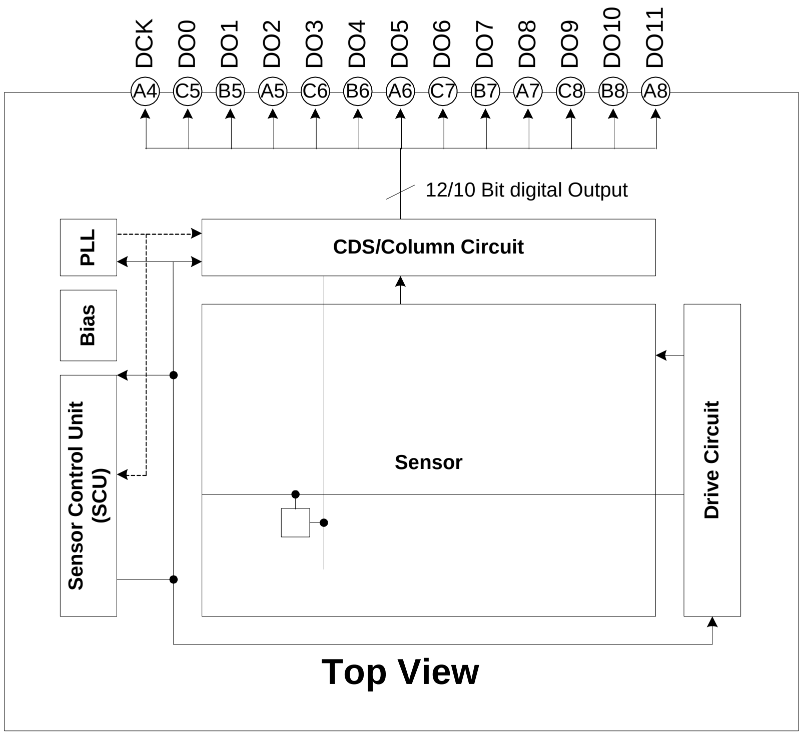
Pixel Arrangement

(Top View)



Pixel Arrangement - Physical Image

Block Diagram and Pin Configuration



Block Diagram

Index mark

	1	2	3	4	5	6	7	8	9	10
A	GND	GND	INCK	DCK	DO2	DO5	DO8	DO11	TEST1	GND
B	VDDL	VDDL	GND	VDDM	DO1	DO4	DO7	DO10	VDDL	GND
C	VDDL	GND	VDDL	GND	DO0	DO3	DO6	DO9	VDDL	GND
D	VDDH	GND	GND	GND	VDDM	VDDM	GND	VDDL	GND	VDDL
E	VDDH	GND	VDDH	GND	GND	GND	GND	SDO	SDI/SDA	XCE
F	GND	VDDH	GND	XCLR	TEST2	VDDM	VDDH	SCK/SCL	XMASTER	TEST3
G	VCAP1	VCAP2	TEST4	XVS	GND	VDDL	GND	TEST5	GND	VDDH
H	GND	VDDH	GND	XHS	VDDL	GND	VDDH	VRL	VCP	GND

Pin Configuration

Pin Description

Pin No.	I/O	Analog /Digital	Symbol	Description	Remarks
A1	GND	D	GND	GND	—
A2	GND	D	GND	GND	—
A3	I	D	INCK	Master Clock	37.125MHz
A4	O	D	DCK	Data clock	—
A5	O	D	DO2	CMOS parallel output	—
A6	O	D	DO5	CMOS parallel output	—
A7	O	D	DO8	CMOS parallel output	—
A8	O	D	DO11	CMOS parallel output	—
A9	D	A	TEST1	TEST pin	Fixed to Low
A10	GND	D	GND	GND	—
B1	Power	D	VDDL	1.2 V power supply	—
B2	Power	D	VDDL	1.2 V power supply	—
B3	GND	D	GND	GND	—
B4	Power	D	VDDM	1.8 V power supply	—
B5	O	D	DO1	CMOS parallel output	—
B6	O	D	DO4	CMOS parallel output	—
B7	O	D	DO7	CMOS parallel output	—
B8	O	D	DO10	CMOS parallel output	—
B9	Power	D	VDDL	1.2 V power supply	—
B10	GND	D	GND	GND	—
C1	Power	D	VDDL	1.2 V power supply	—
C2	GND	D	GND	GND	—
C3	Power	D	VDDL	1.2 V power supply	—
C4	GND	D	GND	GND	—
C5	O	D	DO0	CMOS parallel output	—
C6	O	D	DO3	CMOS parallel output	—
C7	O	D	DO6	CMOS parallel output	—
C8	O	D	DO9	CMOS parallel output	—
C9	Power	D	VDDL	1.2 V power supply	—
C10	GND	D	GND	GND	—
D1	Power	A	VDDH	2.7 V power supply	—
D2	GND	A	GND	GND	—
D3	GND	A	GND	GND	—
D4	GND	D	GND	GND	—
D5	Power	D	VDDM	1.8 V power supply	—
D6	Power	D	VDDM	1.8 V power supply	—
D7	GND	D	GND	GND	—
D8	Power	D	VDDL	1.2 V power supply	—
D9	GND	D	GND	GND	—
D10	Power	D	VDDL	1.2 V power supply	—

Pin No.	I/O	Analog /Digital	Symbol	Description	Remarks
E1	Power	A	VDDH	2.7 V power supply	–
E2	GND	A	GND	GND	–
E3	Power	A	VDDH	2.7 V power supply	–
E4	GND	D	GND	GND	–
E5	GND	D	GND	GND	–
E6	GND	D	GND	GND	–
E7	GND	A	GND	GND	–
E8	O	D	SDO	(4-wire): Serial I/F (register value input) (I^2C): Open	–
E9	I/O	D	SDI/SDA	(4-wire): Serial I/F (register value output) (I^2C): SDA pin	–
E10	I	D	XCE	(4-wire): Serial I/F (Chip enable) (I^2C): Fixed to High	–
F1	GND	A	GND	GND	–
F2	Power	A	VDDH	2.7 V power supply	–
F3	GND	A	GND	GND	–
F4	I	D	XCLR	System clear	–
F5	TEST	D	TEST2	Normal sync mode: Open DCK sync mode: Vertical sync signal	–
F6	Power	D	VDDM	1.8 V power supply	–
F7	Power	A	VDDH	2.7 V power supply	–
F8	I	D	SCK/SCL	(4-wire): Serial I/F (clock input) (I^2C): SCL pin	–
F9	I	D	XMASTER	Slave / Master selection Slave mode: High / Master mode: Low	High: 1.8V Low: GND
F10	TEST	D	TEST3	TEST pin	Fixed to Low
G1	TEST	A	VCAP1	Reference pin	Connect to an external capacitor
G2	TEST	A	VCAP2	Reference pin	Connect to an external capacitor
G3	TEST	A	TEST4	TEST pin	Open
G4	I/O	D	XVS	Vertical sync signal	–
G5	GND	D	GND	GND	–
G6	Power	D	VDDL	1.2 V power supply	–
G7	GND	D	GND	GND	–
G8	TEST	D	TEST5	TEST pin	Fixed to High
G9	GND	A	GND	GND	–
G10	Power	A	VDDH	2.7 V power supply	–
H1	GND	A	GND	GND	–
H2	Power	A	VDDH	2.7 V power supply	–
H3	GND	A	GND	GND	–
H4	I/O	D	XHS	Horizontal sync signal	–
H5	Power	D	VDDL	1.2 V power supply	–
H6	GND	A	GND	GND	–
H7	Power	A	VDDH	2.7 V power supply	–
H8	I	A	VRL	Connect to VCP pin	Connect to an external capacitor
H9	O	A	VCP	Connect to VRL pin	Connect to an external capacitor
H10	GND	D	GND	GND	–

Electrical Characteristics

The electrical characteristics of this device are shown below.

DC Characteristics

Item		Pin	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply voltage	Analog	$V_{DD}H$	AV_{DD}	—	2.6	2.7	2.8	V
	Digital	$V_{DD}M$	OV_{DD}	—	1.7	1.8	1.9	V
		$V_{DD}L$	DV_{DD}	—	1.1	1.2	1.3	V
Digital input voltage		XHS XVS XCLR INCK XMASTER XCE SDI SCK	V_{IH}	XVS/XHS: In slave mode	$0.8OV_{DD}$	—	—	V
			V_{IL}		—	—	$0.2OV_{DD}$	V
Digital output voltage		DO [11:0] DCK	V_{OH}	CMOS output	OV_{DD} – 0.4	—	—	V
			V_{OL}		—	—	0.4	V
		XHS XVS TEST2 SDO	V_{OH}	XVS/XHS: In master mode, CMOS output	OV_{DD} – 0.4	—	—	V
			V_{OL}		—	—	0.4	V

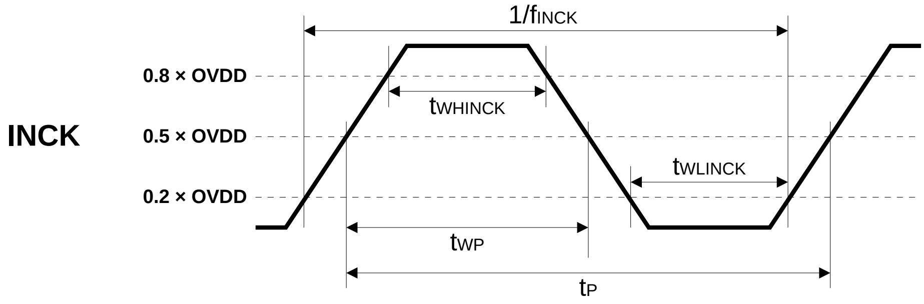
Current Consumption

Item, conditions	Pin	Symbol	Typ.	Max.	Unit
HD1080 p mode 10 bit/12 bit 30 frame/s	$V_{DD}H$	IAV_{DD}	TBD	TBD	mA
	$V_{DD}L$	IDV_{DD}	TBD	TBD	
	$V_{DD}M$	IOV_{DD}	TBD	TBD	
Standby current	$V_{DD}H$	IAV_{DD}_STB	TBD	TBD	µA
	$V_{DD}L$	IDV_{DD}_STB	TBD	TBD	
	$V_{DD}M$	IOV_{DD}_STB	TBD	TBD	

Typ.: AV_{DD} = 2.7 V, OV_{DD} = 1.8 V, DV_{DD} = 1.2 V, Tj = 25 ˚C
Max.: AV_{DD} = 2.8 V, OV_{DD} = 1.9 V, DV_{DD} = 1.3 V, Tj = 60 ˚C
Standard luminous intensity: Luminous intensity at standard imaging condition I
Saturated luminous intensity: Luminous intensity when the sensor is saturated
Standby current: Tj = 60 ˚C, INCK = 0 V

AC Characteristics

Master clock (INCK)

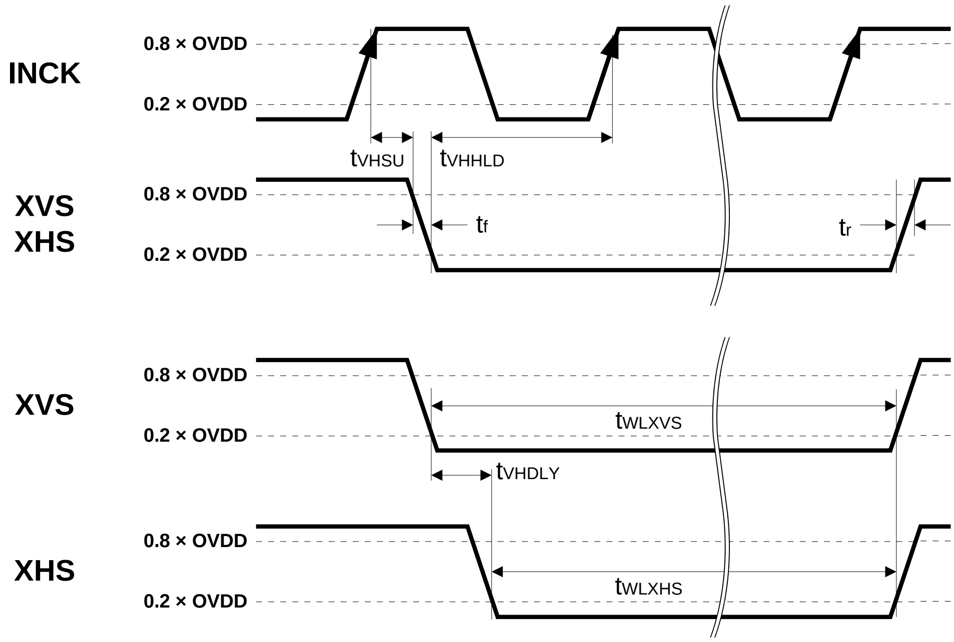


Duty Ratio = tWP / tP × 100

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
INCK clock frequency	f_{INCK}	*1	37.125	*1	MHz	
INCK Low level width	t_{WLINCK}	10.3	—	—	ns	
INCK High level width	t_{WHINCK}	10.3	—	—	ns	
INCK clock duty	—	45	50	55	%	Defined with 0.5 × OV_{DD}

*1 The INCK fluctuation affects the frame rate. The sensor does not operate with specified frame rate except for typical value.

XVS and XHS Input Characteristics (In Slave Mode)

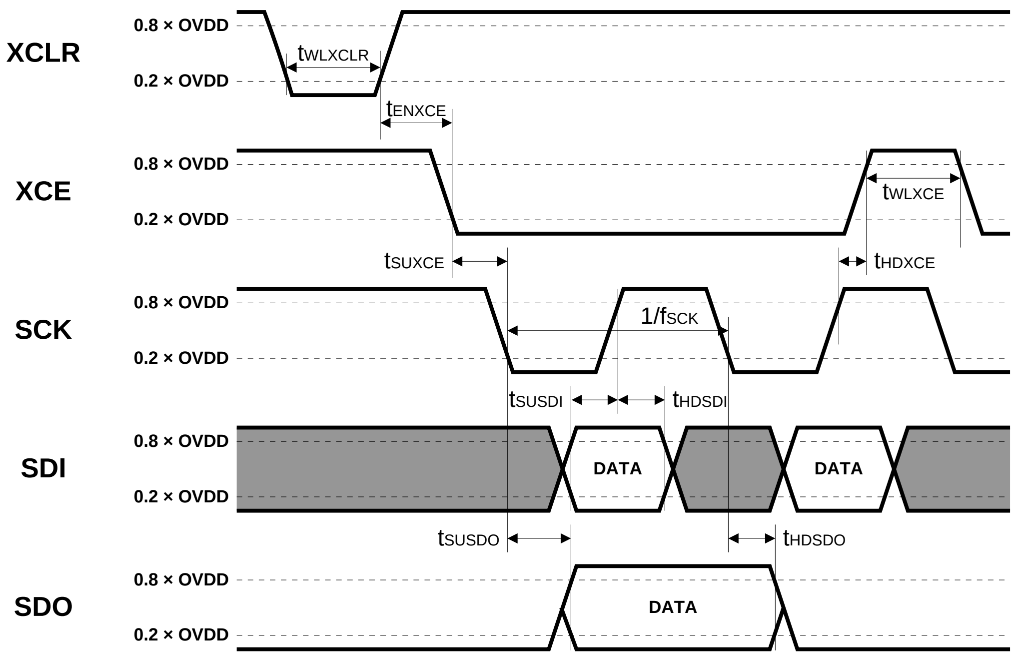


Item	Symbol	Min.	Typ.	Max.	Unit
XVS fall time	tf	—	—	5	ns
XVS rise time	tr	—	—	5	ns
XHS fall time	tf	—	—	5	ns
XHS rise time	tr	—	—	5	ns
XVS, XHS input setup time	t_{VHSU}	0	—	—	ns
XVS, XHS input hold time	t_{VHHLD}	5	—	—	ns
XVS Low level pulse width	t_{WLXVS}	4	—	100	INCK
XHS Low level pulse width	t_{WLXHS}	4	—	100	INCK
XVS-XHS fall delay	t_{VHDLY}	—	—	1	INCK

XVS, XHS Output Characteristics (In Master Mode)

* XVS and XHS cannot be used for the sync signal to pixels. Be sure to detect sync code to detect the start of effective pixels in 1 line. For the output waveforms in master mode, see the item of “Slave Mode and Master Mode”

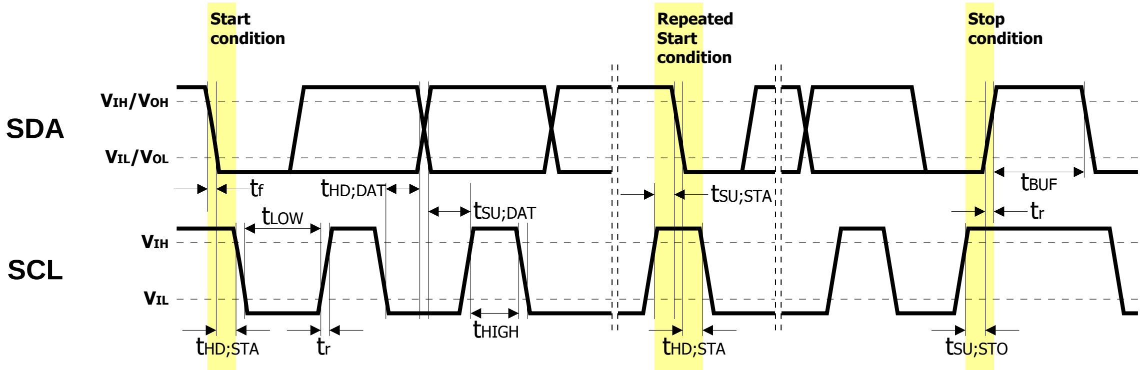
Serial Communication (4-wire Serial)



(Output load capacitance: 8 pF)

Item	Symbol	Min.	Typ.	Max.	Unit
SCK clock frequency	f_{SCK}	—	13.5	—	MHz
XCLR Low level pulse width	t_{WLXCLR}	500	—	—	ns
XCE effective margin	t_{ENXCE}	100	—	—	ns
XCE input setup time	t_{SUXCE}	20	—	—	ns
XCE input hold time	t_{HDXCE}	20	—	—	ns
XCE High level pulse width	t_{WLXCE}	20	—	—	ns
SDI input setup time	t_{SUSDI}	10	—	—	ns
SDI input hold time	t_{HDSDI}	10	—	—	ns
SDO output setup time	t_{SUSDO}	—	—	25	ns
SDO output hold time	t_{HDSDO}	0	—	—	ns

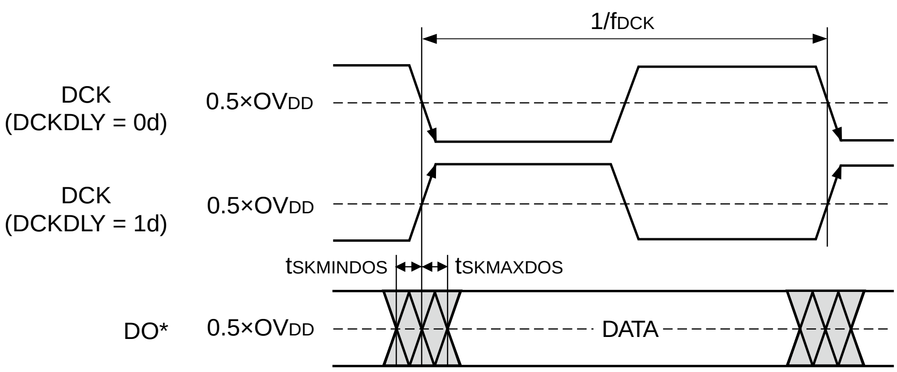
Serial Communication (I^2C)



Item	Symbol	Standard mode		Fast mode		Unit
		Min.	Max.	Min.	Max.	
(SCL・SDA) Low level input voltage	V_{IL}	-0.3	-0.2OV$_{DD}$	-0.3	0.2OV$_{DD}$	V
(SCL・SDA) High level input voltage	V_{IH}	0.8OV$_{DD}$	1.9	0.8OV$_{DD}$	1.9	V
(SDA) Low level output voltage	V_{CL}	0	0.2OV$_{DD}$	0	0.2OV$_{DD}$	V
(SDA) High level output voltage	V_{CH}	0.8OV$_{DD}$	—	0.8OV$_{DD}$	—	V

Item	Symbol	Standard mode		Fast mode		Unit
		Min.	Max.	Min.	Max.	
SCL clock frequency	f_{SCL}	0	100	0	400	kHz
Hold time (start condition)	$t_{HD;STA}$	0.4	—	0.6	—	µs
Low level of the SCL clock	t_{LOW}	4.7	—	1.3	—	µs
High level of the SCL clock	t_{HIGH}	4.0	—	0.6	—	µs
Setup time (rep.-start condition)	$t_{SU;STA}$	4.7	—	0.6	—	µs
Data hold time	$t_{HD;DAT}$	3	3450	3	900	ns
Data setup time	$t_{SU;DAT}$	250	—	100	—	ns
Rise time (SDA and SCL)	t_r	—	1000	20+0.1C$_b$	300	ns
Fall time (SDA and SCL)	t_f	—	300	20+0.1C$_b$	300	ns
Setup time (stop condition)	$t_{SU;STO}$	4.0	—	0.6	—	µs
Bus free time between	t_{BUF}	4.7	—	1.3	—	µs
Stop and Start condition	C_b	—	400	—	400	pF

DCK and DO Output Characteristics



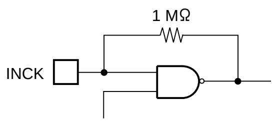
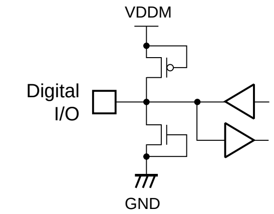
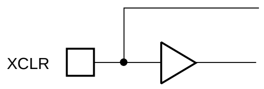
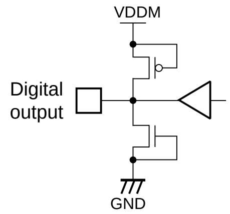
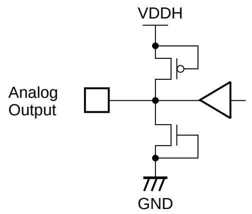
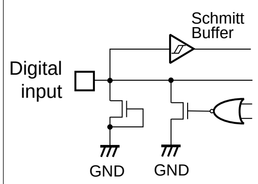
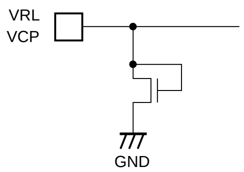
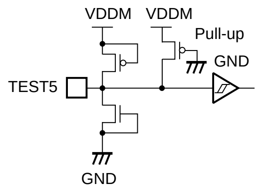
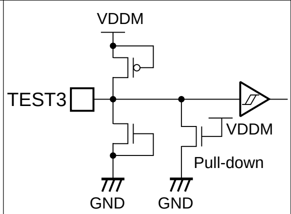
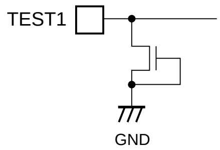
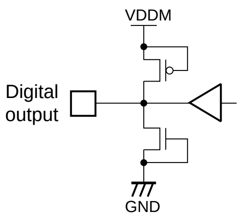
(Output load capacitance: 8 pF)

Item	Symbol	Min..	Typ.	Max.	Unit
DCK clock frequency	f_{DCK}	—	INCK	—	MHz
DCK clock duty	—	40	50	60	%
Maximum skew between DCK and DO*	$t_{SKMAXDOS}$	—	—	2	ns
Minimum skew between DCK and DO*	$t_{SKMINDOS}$	—	—	2	ns

The DCK frequency is the same as that of INCK when the FRSEL is set to 1.

I/O Equivalent Circuit Diagram

□ : External pin

Symbol	Equivalent circuit	Symbol	Equivalent circuit
INCK		XVS/XHS	
XCLR		SDO	
TEST4 Vcap1 Vcap2		SDI SCK XCE	
VRL VCP		TEST5	
TEST3		TEST1	
DOx DCK			

Spectral Sensitivity Characteristics

(Excludes lens characteristics and light source characteristics.)

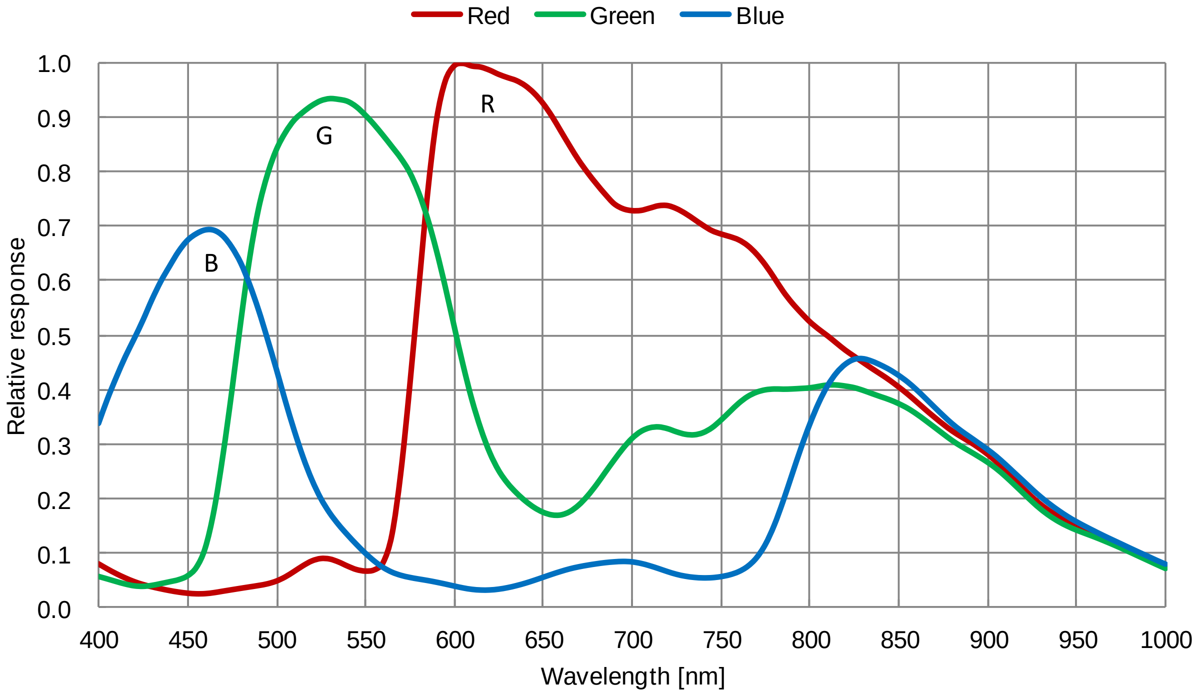


Image Sensor Characteristics

(AV_{DD} = 2.7 V, OV_{DD} = 1.8 V, DV_{DD} = 1.2 V, Tj = 60 °C, HD1080p 12-bit 30frame/s, Gain: 0 dB)

Item		Symbol	Min.	Typ.	Max.	Unit	Measurement method	Remarks
G sensitivity		Sg	TBD (TBD)	3239 (510)	—	Digit (mV)	1	1/30 s integration
Sensitivity ratio	R/G	Rr	TBD	—	TBD	—	2	—
	B/G	Rb	TBD	—	TBD	—		
Saturation signal	Zone0-II'*3	Vsat2D	4095 (645)	—	—	Digit (mV)	3	Tj = 60 °C
Video signal shading	Zone0-II'*3	SH2D	—	—	TBD	%	4	—

*1 Conversion is executed with 1 digit = 0.630 mV for 10-bit output and 1 digit = 0.1575 mV for 12-bit output.
*2 The video signal shading is the measured value in the wafer status (including color filter) and does not include the seal glass characteristics.
*3 See the Zone Definition of Video Signal Shading (diagram below) for Zone.

Zone Definition of Video Signal Shading

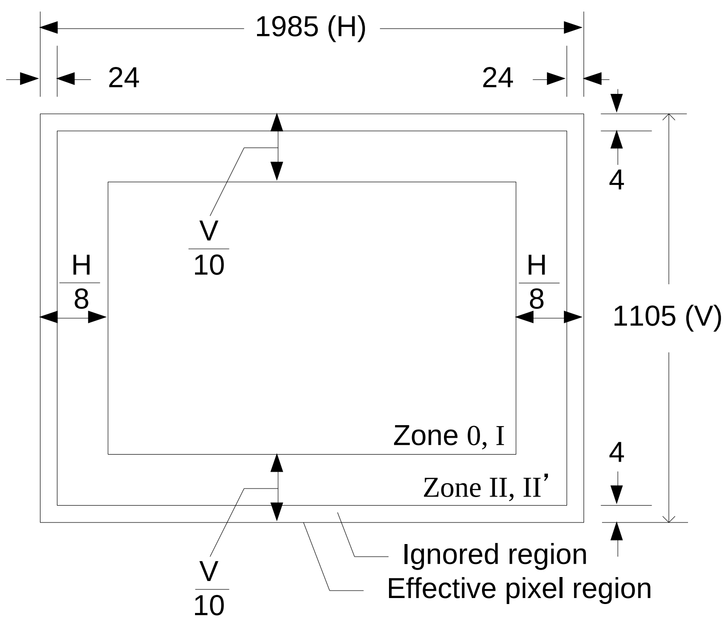


Image Sensor Characteristics Measurement Method

Measurement Conditions

In the following measurements, the device drive conditions are at the typical values of the bias conditions and clock voltage conditions.
In the following measurements, spot pixels are excluded and, unless otherwise specified, the optical black (OB) level is used as the reference for the signal output, which is taken as the value of the Gr/Gb channel signal output or the R/B channel signal output of the measurement system.

Color Coding of this Image Sensor and Readout

The primary color filters of this image sensor are arranged in the layout shown in the figure below. Gr and Gb represent the G signal on the same line as the R and B signals, respectively. The Gb signal and B signal lines and the R signal and Gr signal lines are output successively.

Gb	B	Gb	B
R	Gr	R	Gr
Gb	B	Gb	B
R	Gr	R	Gr

Color Coding Diagram

Definition of standard imaging conditions

◆ Standard imaging condition I:

Use a pattern box (luminance: 706 cd/m^2, color temperature of 3200 K halogen source) as a subject. (Pattern for evaluation is not applicable.) Use a testing standard lens with CM500S (t = 1.0 mm) as an IR cut filter and image at F5.6. The luminous intensity to the sensor receiving surface at this point is defined as the standard sensitivity testing luminous intensity.

◆ Standard imaging condition II:

Image a light source (color temperature of 3200 K) with a uniformity of brightness within 2 % at all angles. Use a testing standard lens with CM500S (t = 1.0 mm) as an IR cut filter. The luminous intensity is adjusted to the value indicated in each testing item by the lens diaphragm.

◆ Standard imaging condition III:

Image a light source (color temperature of 3200 K) with a uniformity of brightness within 2 % at all angles. Use a testing standard lens (exit pupil distance -30 mm) with CM500S (t = 1.0 mm) as an IR cut filter. The luminous intensity is adjusted to the value indicated in each testing item by the lens diaphragm.

Measurement Method

1. Sensitivity

   Set the measurement condition to the standard imaging condition I. After setting the electronic shutter mode with a shutter speed of 1/100 s, measure the Gr and Gb signal outputs (VGr, VGb) at the center of the screen, and substitute the values into the following formula.

   $$Sg = (VGr + VGb) / 2 \times 100 / 30 \text{ [mV]}$$

2. Sensitivity ratio

   Set the measurement condition to the standard imaging condition II. After adjusting the average value of the Gr and Gb signal outputs to 464 mV, measure the R signal output (VR [mV]), the Gr and Gb signal outputs (VGr, VGb [mV]) and the B signal output (VB [mV]) at the center of the screen in frame readout mode, and substitute the values into the following formulas.

   $$VG = (VGr + VGb) / 2$$
   $$Rr = VR / VG$$
   $$Rb = VB / VG$$

3. Saturation signal

   Set the measurement condition to the standard imaging condition II. After adjusting the luminous intensity to 20 times the intensity with the average value of the Gr and Gb signal outputs, 464 mV, measure the average values of the Gr, Gb, R and B signal outputs.

4. Video signal shading

   Set the measurement condition to the standard imaging condition III. With the lens diaphragm at F2.8, adjust the luminous intensity so that the average value of the Gr and Gb signal outputs is 464 mV. Then measure the maximum value (Gmax [mV]) and the minimum value (Gmin [mV]) of the Gr and Gb signal outputs, and substitute the values into the following formula.

   $$SH = (Gmax – Gmin) / 464 \times 100 \text{ [\%]}$$

Setting Registers with Serial Communication

This sensor can write and read the setting values of the various registers shown in the Register Map by 4-wire serial communication and I^{2}C communication. See the Register Map for the addresses and setting values to be set. Because the two communication systems are judged at the first communication, once they are judged, the communication cannot be switched until sensor reset. The pin for 4-wire serial communication and I^{2}C communication is shared, so the external pin XCE must be fixed to power supply side when using I^{2}C communication.

Some functions are set by different register according to communication method (4-wire / I^{2}C).

Description of Setting Registers (4-wire)

The serial data input order is LSB-first transfer. The table below shows the various data types and descriptions.

Serial Data Transfer Order

Chip ID	Start address	Data	Data	Data	···
(8 bit)	(8 bit)	(8 bit)	(8 bit)	(8 bit)	(8 bit)

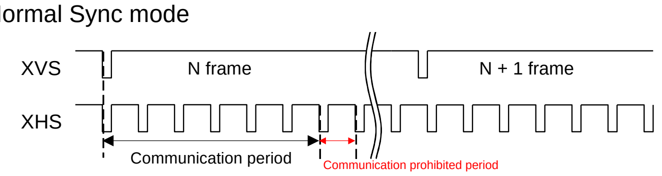
Type and Description

Type	Description
ChipID	02h: Write to the CID = 02h register 03h: Write to the CID = 03h register 82h: Read from the CID = 02h register 83h: Read from the CID = 03h register
Address	Designate the address according to the Register Map. When using a communication method that designates continuous addresses, the address is automatically incremented from the previously transmitted address.
Data	Input the setting values according to the Register Map.

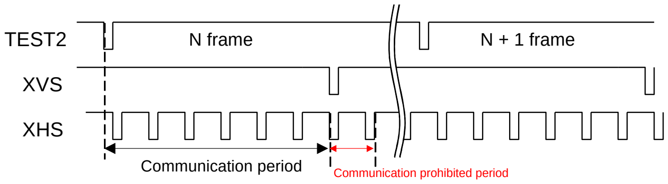
Register Communication Timing

Perform register communication within the 6H period as shown in the figure below. Register setting values are reflected at the following timing. When communication is performed during the communication period shown in the figure below, items noted as "V" in the "Reflection timing" column of the Register Map are output in the state with the setting value reflected in the N frame. However, note that although the integration time setting is reflected in the N frame, it is reflected to shutter control after N frame readout, so the setting value is reflected to the output in the N + 1 frame. Items that are reflected instantly are reflected at the timing when communication is performed.

Normal Sync mode



DCK Sync mode



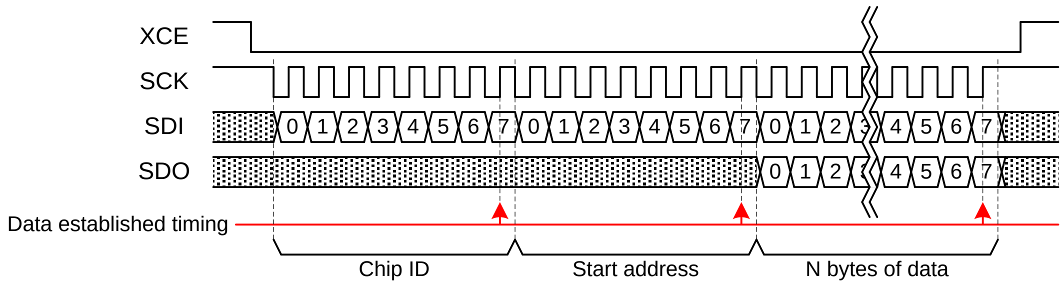
Register Reflection Timing

Register Write and Read

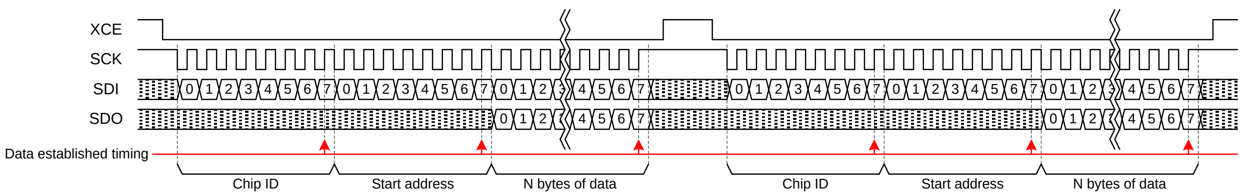
- Follow the communication procedure below when writing registers.
  (1) Set XCE Low to enable the chip's communication function. Serial data input is executed using SCK and SDI.
  (2) Transmit data in sync with SCK 1 bit at a time from the LSB using SDI. Transfer SDI in sync with the falling edge of SCK. (The data is loaded at the rising edge of SCK.)
  (3) Input the Chip ID (CID = 02h or 03h) to the first byte. If the Chip ID differs, subsequent data is ignored.
  (4) Input the start address to the second byte. The address is automatically incremented.
  (5) Input the data to the third and subsequent bytes. The data in the third byte is written to the register address designated by the second byte, and the register address is automatically incremented thereafter when writing the data for the fourth and subsequent bytes. Normal register data is loaded to the inside of the sensor and established in 8-bit units.
  (6) The register values starting from the register address designated by the second byte are output from the SDO pin. The register values before the write operation are output. The actual register values are the input data.
  (7) Set XCE High to end communication.

- Follow the communication procedure below when reading registers.
  (1) Set XCE Low to enable the chip's communication function. Serial data input is executed using SCK and SDI.
  (2) Transmit data in sync with SCK 1 bit at a time from the LSB using SDI. Transfer SDI in sync with the falling edge of SCK. (The data is loaded at the rising edge of SCK.)
  (3) Input Chip ID (CID = 82h or 83h) to the first byte. If the Chip ID differs, subsequent data is ignored.
  (4) Input the start address to the second byte. The address is automatically incremented.
  (5) Input data to the third and subsequent bytes. Input dummy data in order to read the registers. The dummy data is not written to the registers. To read continuous data, input the necessary number of bytes of dummy data.
  (6) The register values starting from the register address designated by the second byte are output from the SDO pin. The input data is not written, so the actual register values are output.
  (7) Set XCE High to end communication.

Note) Even when changing register setting values during imaging, communication should finish within the 6H communication period. When writing data to multiple registers with discontinuous addresses, access to undesired registers can be avoided by repeating the above procedure multiple times. The figures on the following page show examples of transmission.



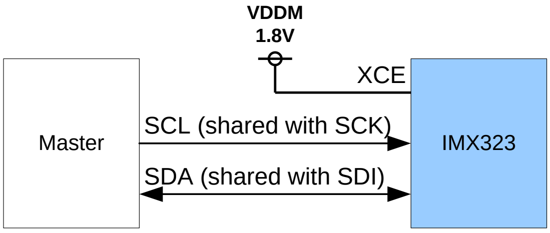
Communication Timing to Registers with Continuous Addresses



Communication Timing to Registers with Discontinuous Addresses

Description of Setting Registers (I^2C)

The serial data input order is MSB-first transfer. The table below shows the various data types and descriptions.



Pin connection of serial communication

Slave address

MSB							LSB
0	0	1	1	0	1	0	R/W

*R / W is data direction bit

R / W

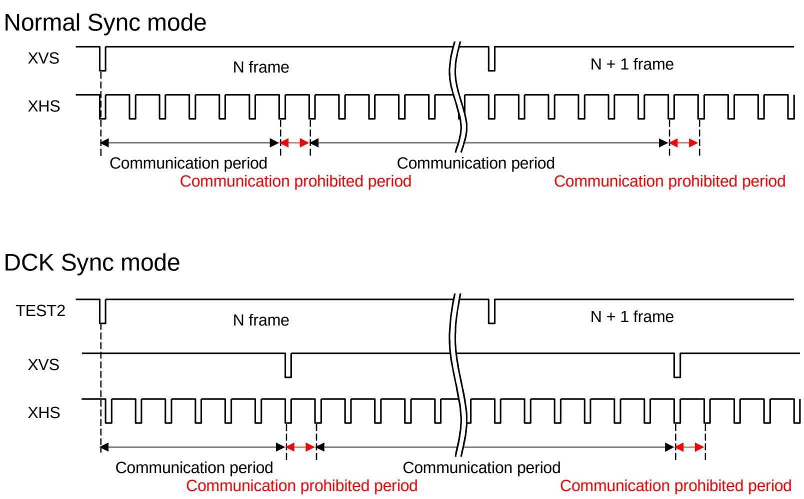
R / W	Data direction
0	Write (Master → Sensor)
1	Read (Sensor → Master)

I^2C pin description

Symbol	Pin No.	Description
SDA (common to SDI)	E9	Serial data communication
SCL (common to SCK)	F8	Serial clock input

Register Communication Timing

Perform register communication within the communication period shown below. Register setting values are reflected at the following timing. When communication is performed during the communication period shown in the figure below, items noted as “V” in the “Reflection timing” column of the Register Map are output in the state with the setting value reflected in the N frame. However, note that although the integration time setting is reflected in the N frame, it is reflected to shutter control after N frame readout, so the setting value is reflected to the output in the N + 1 frame. Items that are reflected instantly are reflected at the timing when communication is performed.



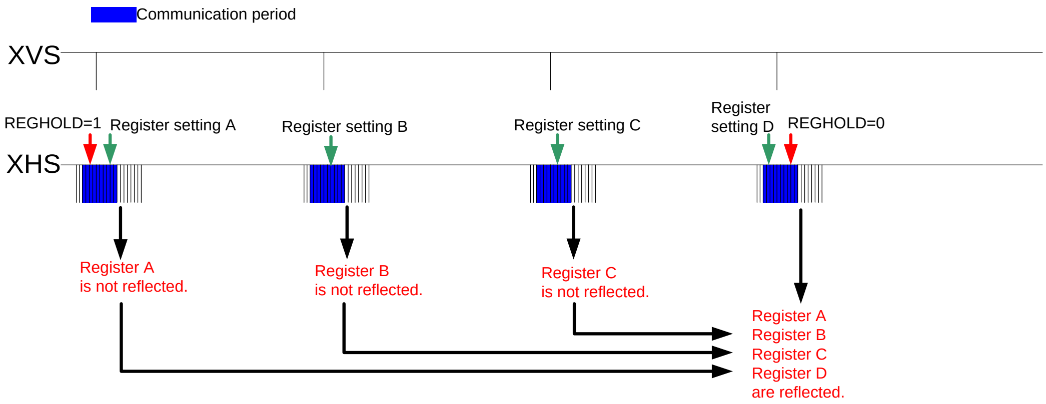
Register Reflection Timing

Register Hold Setting

Register setting can be transmitted with divided to several frames and it can be reflected globally at a certain frame by the register REGHOLD (address: 0104h [0]). Setting REGHOLD = 1 at the start of register communication period prevents the registers that are set thereafter from reflecting at the frame reflection timing. The registers that are set when setting REGHOLD = 1 are reflected globally by setting REGHOLD = 0 at the end of communication period of the desired frame to reflect the register.

Register hold register

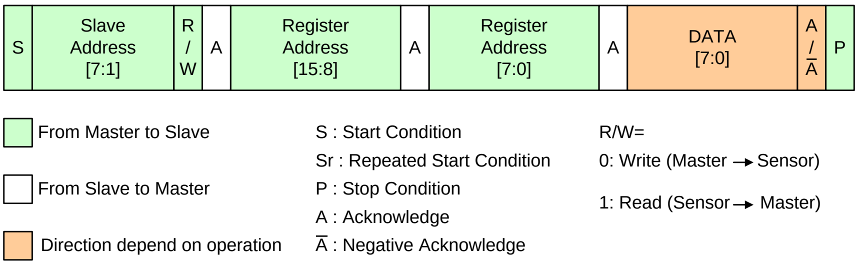
Register details			Initial value	Setting value
Register name	Address	bit		
REGHOLD	0104h	[0]	1	0h: Invalid 1h: Valid (register hold)



Register Hold Setting

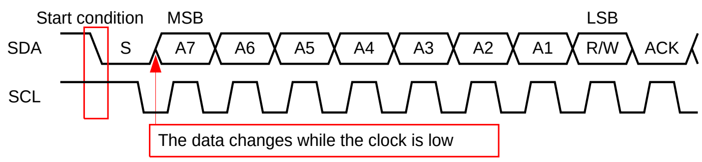
Communication Protocol

I²C serial communication supports a 16-bit register address and 8-bit data message type.

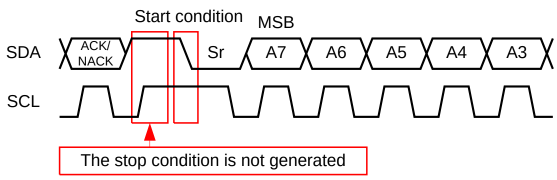


Communication protocol

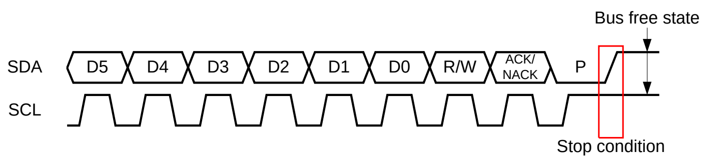
Data is transferred serially, MSB first in 8-bit units. After each data byte is transferred, A (Acknowledge) / $\overline{A}$ (Negative Acknowledge) is transferred. Data (SDA) is transferred at the clock (SDL) cycle. SDA can change only while SCL is Low, so the SDA value must be held while SCL is High. The Start condition is defined by SDA changing from High to Low while SCL is High. When the Stop condition is not generated in the previous communication phase and Start condition for the next communication is generated, that Start condition is recognized as a Repeated Start condition.



Start Condition

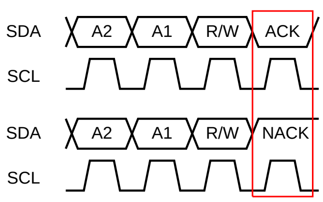


Repeated Start Condition



Stop Condition

After transfer of each data byte, the Master or the sensor transmits an Acknowledge / Negative Acknowledge and release (does not drive) SDA. When Negative Acknowledge is generated, the Master must immediately generate the Stop Condition and end the communication.

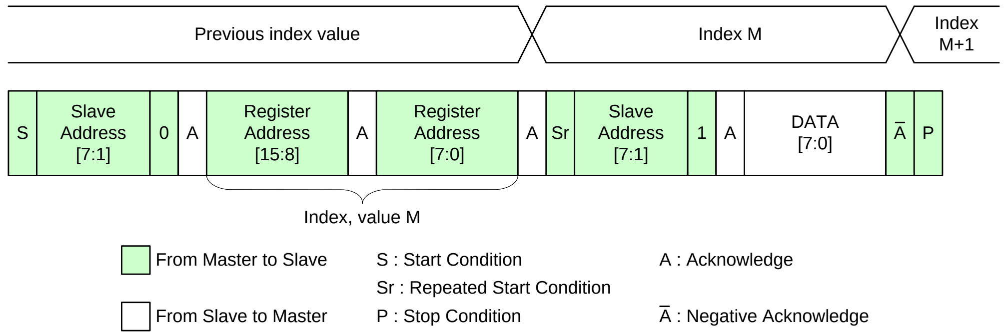


Acknowledge and Negative Acknowledge

Register Write and Read in I²C Communication

Single Read from Random Location

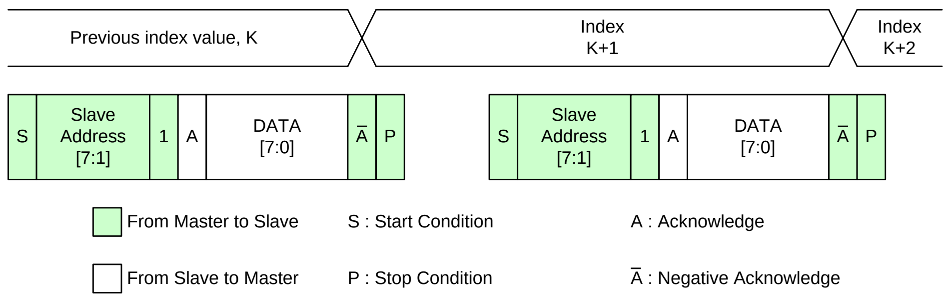
The sensor has an index function that indicates which address it is focusing on. In reading the data at an optional single address, the Master must set the index value to the address to be read. For this purpose it performs dummy write operation up to the register address. The upper level of the figure below shows the sensor internal index value, and the lower level of the figure shows the SDA I/O data flow. The Master sets the sensor index value to M by designating the sensor slave address with a write request, then designating the address (M). Then, the Master generates the start condition. The Start Condition is generated without generating the Stop Condition, so it becomes the Repeated Start Condition. Next, when the Master sends the slave address with a read request, the sensor outputs an Acknowledge immediately followed by the index address data on SDA. After the Master receives the data, it generates a Negative Acknowledge and the Stop Condition to end the communication



Single Read from Random Location

Single Read from Current Location

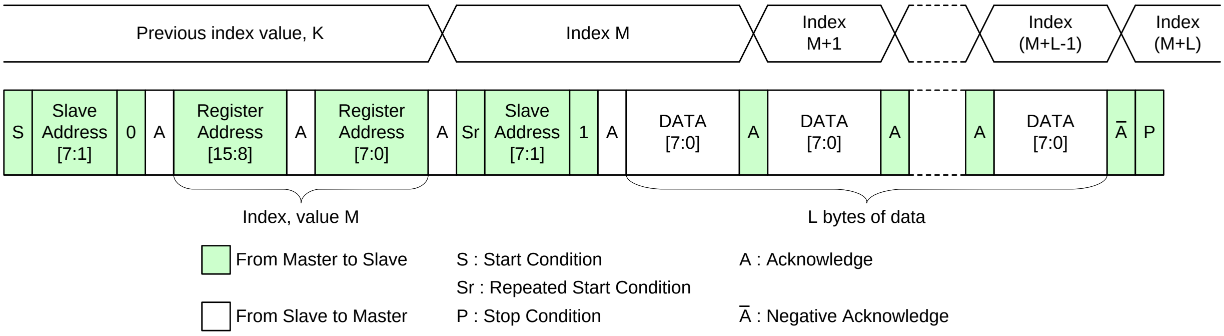
After the slave address is transmitted by a write request, that address is designated by the next communication and the index holds that value. In addition, when data read / write is performed, the index is incremented by the subsequent Acknowledge / Negative Acknowledge timing. When the index value is known to indicate the address to be read, sending the slave address with a read request allows the data to be read immediately after Acknowledge. After receiving the data, the Master generates a Negative Acknowledge and the Stop Condition to end the communication, but the index value is incremented, so the data at the next address can be read by sending the slave address with a read request.



Single Read from Current Location

Sequential Read Starting from Random Location

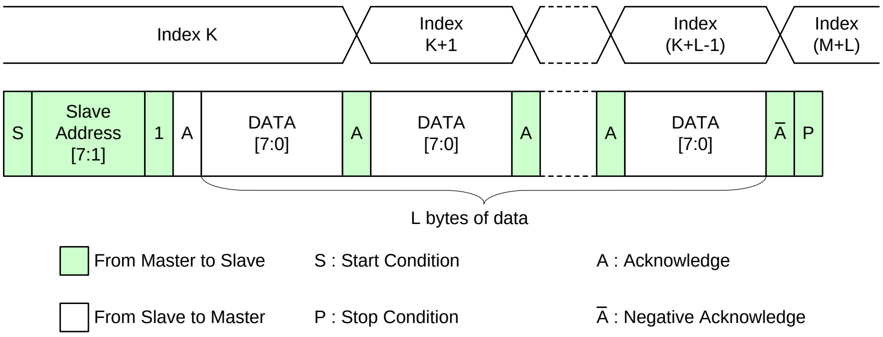
In reading data sequentially, which is starting from an optional address, the Master must set the index value to the start of the addresses to be read. For this purpose, dummy write operation includes the register address setting. The Master sets the sensor index value to M by designating the sensor slave address with a read request, then designating the address (M). Then, the Master generates the Repeated Start Condition. Next, when the Master sends the slave address with a read request, the sensor outputs an Acknowledge followed immediately by the index address data on SDA. When the Master outputs an Acknowledge after it receives the data, the index value inside the sensor is incremented and the data at the next address is output on SDA. This allows the Master to read data sequentially. After reading the necessary data, the Master generates a Negative Acknowledge and the Stop Condition to end the communication.



Sequential Read Starting from Random Location

Sequential Read Starting from Current Location

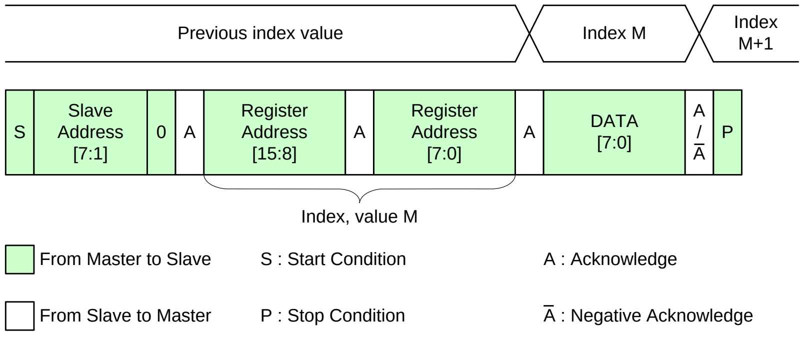
When the index value is known to indicate the address to be read, sending the slave address with a read request allows the data to be read immediately after the Acknowledge. When the Master outputs an Acknowledge after it receives the data, the index value inside the sensor is incremented and the data at the next address is output on SDA. This allows the Master to read data sequentially. After reading the necessary data, the Master generates a Negative Acknowledge and the Stop Condition to end the communication.



Sequential Read Starting from Current Location

Single Write to Random Location

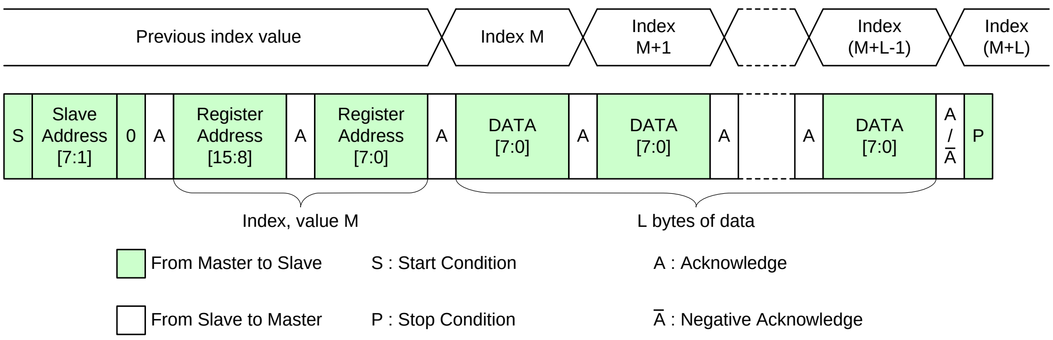
The Master sets the sensor index value to M by designating the sensor slave address with a write request, and designating the address (M). After that the Master can write the value in the designated register by transmitting the data to be written. After writing the necessary data, the Master generates the Stop Condition to end the communication.



Single Write to Random Location

Sequential Write Starting from Random Location

The Master can write a value to register address M by designating the sensor slave address with a write request, designating the address (M), and then transmitting the data to be written. After the sensor receives the write data, it outputs an Acknowledge and at the same time increments the register address, so the Master can write to the next address simply by continuing to transmit data. After the Master writes the necessary number of bytes, it generates the Stop Condition to end the communication.



Sequential Write Starting from Random Location

Register Map

There are some functions that address is change according to communication method. When described as (I^2C), this function will be enabled by I^2C communication. When described as (4-wire), this function will be enabled by 4-wire communication.

I^2C only

Address	bit	Register name	Description	Default value after reset: By register	Default value after reset: By address	Reflection timing
0000h to 0007h	[7:0] to [7:0]		Do not rewrite.	—	—	—
0008h	[0]	I^2C BLKLEVEL [8]	Black level offset value setting (I^2C)	040h	0h	Immediately
0009h	[7:0]	I^2C BLKLEVEL [7:0]			40h	
000Ah to 00FFh	[7:0] to [7:0]		Do not rewrite.	—	—	–
0100h	[0]	MODE_SEL	Standby control (I^2C) 0: Standby 1: Normal operation	0h	00h	*1
	[1]		Fixed to 0	0h		—
	[2]		Fixed to 0	0h		—
	[3]		Fixed to 0	0h		—
	[4]		Fixed to 0	0h		—
	[5]		Fixed to 0	0h		—
	[6]		Fixed to 0	0h		—
	[7]		Fixed to 0	0h		—
0101h	[0]	IMG_ORIENTATION_H	Horizontal (H) scanning direction control (I^2C) 0: Normal 1: Inverted	0h	00h	V
	[1]	IMG_ORIENTATION_V	Vertical (V) scanning direction control (I^2C) 0: Normal 1: Inverted	0h		V
	[2]		Fixed to 0	0h		—
	[3]		Fixed to 0	0h		—
	[4]		Fixed to 0	0h		—
	[5]		Fixed to 0	0h		—
	[6]		Fixed to 0	0h		—
	[7]		Fixed to 0	0h		—
0102h to 0103h	[7:0] to [7:0]		Do not rewrite.	—	—	—

Address	bit	Register name	Description	Default value after reset By register	Default value after reset By address	Reflection timing
0104h	[0]	REG_HOLD	Register reflection timing hold 0: Normal communication mode. When register setting is hold, reflection is applied. 1: Register setting hold	0h	00h	Immediately
	[1]		Fixed to 0	0h		—
	[2]		Fixed to 0	0h		—
	[3]		Fixed to 0	0h		—
	[4]		Fixed to 0	0h		—
	[5]		Fixed to 0	0h		—
	[6]		Fixed to 0	0h		—
	[7]		Fixed to 0	0h		—
0105h to 0111h	[7:0] to [7:0]		Do not rewrite.	—	—	—
0112h	[7:0]	I^2C ADRES1 [7:0]	AD gradation setting (I^2C) 0Ah: 10 bits, 0Ch: 12 bits	0Ah	0Ah	V
0113h	[7:0]	I^2C ADRES2 [7:0]	AD gradation setting (I^2C) 0Ah: 10 bits, 0Ch: 12 bits	0Ah	0Ah	V
0114h to 0201h	[7:0] to [7:0]		Do not rewrite.	—	—	—
0202h	[7:0]	INTEG_TIME [15:8]	Integration time adjustment (I^2C) Designated in line units	0000h	00h	V
0203h	[7:0]	INTEG_TIME [7:0]			00h	
0204h to 033Fh	[7:0] to [7:0]		Do not rewrite.	—	—	—
0340h	[7:0]	FRM_LENGTH [15:8]	In master mode. Vertical (V) direction line number designation (I^2C)	04E2h	04h	V
0341h	[7:0]	FRM_LENGTH [7:0]			E2h	
0342h	[7:0]	LINE_LENGTH [15:8]	In master mode. Horizontal (H) direction clock number designation (I^2C)	044Ch	04h	V
0343h	[7:0]	LINE_LENGTH [7:0]			4Ch	
0344h to 2FFFh	[7:0] to [7:0]		Do not rewrite.	—	—	—

*Fixed the empty bit of 0008h, 0009h to “0”.

Chip ID: 02h

Address		bit	Register name	Description	Default value after reset		Reflection timing
4-wire	I^2C				By register	By address	
00h	3000h	[0]	STANDBY	STANDBY control (4-wire) 0h: Normal operation 1h: STANDBY	1h	01h	*1
		[1]		Fixed to “0”.	0h		—
		[2]		Fixed to “0”.	0h		—
		[3]		Fixed to “0”.	0h		—
		[4]	TESTEN [1:0]	Register write 0h: Invalid 3h: Valid Others: Invalid	0h		Immediately
		[5]					
		[6]		Fixed to “0”.	0h		—
		[7]		Fixed to “0”.	0h		—
01h	3001h	[0]	VREVERSE	Vertical (V) scanning direction control (4-wire) 0: Normal 1: Inverted	0h	00h	V
		[1]	HREVERSE	Horizontal (H) scanning direction control (4-wire) 0: Normal 1: Inverted	0h		—
		[2]		Fixed to “0”.	0h		—
		[3]		Fixed to “0”.	0h		—
		[4]		Fixed to “0”.	0h		—
		[5]		Fixed to “0”.	0h		—
		[6]		Fixed to “0”.	0h		—
		[7]		Fixed to “0”.	0h		—
02h	3002h	[0]	MODE [3:0]	Readout mode designation 1h:HD720 p Fh: HD1080 p Others: Invalid	0h	00h	V
		[1]					
		[2]					
		[3]					
		[4]		Fixed to “0”.	0h		—
		[5]		Fixed to “0”.	0h		—
		[6]		Fixed to “0”.	0h		—
		[7]		Fixed to “0”.	0h		—
03h	3003h	[0]	HMAX [13:0]	LSB In master mode Horizontal (H) direction clock number designation (4-wire) MSB	044Ch	4Ch	V
		[1]					
		[2]					
		[3]					
		[4]					
		[5]					
		[6]					
		[7]					
04h	3004h	[0]				04h	
		[1]					
		[2]					
		[3]					
		[4]					
		[5]					
		[6]		Fixed to “0”.	0h		—
		[7]		Fixed to “0”.	0h		—

Address		bit	Register name	Description	Default value after reset		Reflection timing
4-wire	I^2C				By register	By address	
05h	3005h	[0]	VMAX [15:0]	LSB	04E2h	E2h	V
		[1]					
		[2]					
		[3]					
		[4]					
		[5]					
		[6]		In master mode			
		[7]		Vertical (V) direction line number designation (4-wire)			
06h	3006h	[0]				04h	
		[1]					
		[2]					
		[3]					
		[4]					
		[5]					
		[6]					
		[7]		MSB			
07h	3007h	[7:0]		Fixed to “00h”	00h	00h	—
08h	3008h	[0]	SHS1[15:0]	LSB	0000h	00h	V
		[1]					
		[2]					
		[3]					
		[4]					
		[5]					
		[6]		Integration time adjustment			
		[7]		Designated in line units (4-wire)			
09h	3009h	[0]				00h	
		[1]					
		[2]					
		[3]					
		[4]					
		[5]					
		[6]					
		[7]		MSB			
0Ah	300Ah	[7:0]		Fixed to “00h”	00h	00h	—
0Bh	300Bh	[7:0]		Fixed to “00h”	00h	00h	—
0Ch	300Ch	[7:0]		Fixed to “00h”	00h	00h	—
0Dh	300Dh	[7:0]		Fixed to “00h”	00h	00h	—
0Eh	300Eh	[7:0]		Fixed to “00h”	00h	00h	—
0Fh	300Fh	[7:0]		Fixed to “00h”	00h	00h	—
10h	3010h	[7:0]		Fixed to “00h”	00h	00h	—

Address 4-wire	Address I²C	bit	Register name	Description	Default value after reset By register	Default value after reset By address	Reflection timing
11h	3011h	[0]	FRSEL [2:0]	Output data rate designation 0: 2 times INCK 1: Equal to INCK Others: Invalid	0h	00h	V
		[1]					
		[2]					
		[3]		Fixed to “0”.	0h		—
		[4]		Fixed to “0”.	0h		—
		[5]		Fixed to “0”.	0h		—
		[6]		Fixed to “0”.	0h		—
		[7]		Fixed to “0”.	0h		—
12h	3012h	[0]	SSBRK	Low-speed shutter forcible termination	0h	80h	Immediately
		[1]	ADRES	AD gradation setting (4-wire) 0: 10 bits, 1: 12 bits	0h		V
		[2]		Fixed to “0”.	0h		—
		[3]		Fixed to “0”.	0h		—
		[4]		Fixed to “0”.	0h		—
		[5]		Fixed to “0”.	0h		—
		[6]		Fixed to “0”.	0h		—
		[7]		Fixed to “1”.	1h		—
13h	3013h	[7:0]		Fixed to “40h”.	40h	40h	Immediately
14h	3014h	[7:0]		Fixed to “00h”	00h	00h	—
15h	3015h	[7:0]		Fixed to “00h”	00h	00h	—
16h	3016h	[7:0]		HD1080p: 3Ch HD720p: F0h	00h	00h	V
17h	3017h	[7:0]		Fixed to “00h”	00h	00h	—
18h	3018h	[7:0]		Fixed to “00h”	00h	00h	—
19h	3019h	[7:0]		Fixed to “00h”	00h	00h	—
1Ah	301Ah	[7:0]		Fixed to “00h”	00h	00h	—
1Bh	301Bh	[7:0]		Fixed to “00h”	00h	00h	—
1Ch	301Ch	[7:0]		Fixed to “50h”	50h	50h	—
1Dh	301Dh	[7:0]		Fixed to “00h”	00h	00h	—

Address 4-wire	Address I2C	bit	Register name	Description	Default value after reset By register	Default value after reset By address	Reflection timing
1Eh	301Eh	[0]	GAIN [7:0]	LSB	00h	00h	V
		[1]		Gain setting			
		[2]					
		[3]					
		[4]					
		[5]					
		[6]					
		[7]		MSB			
1Fh	301Fh	[7:0]		Fixed to “73h”.*2	31h	31h	—
20h	3020h	[0]	BLKLEVEL [8:0]	LSB	03Ch	3Ch	Immediately
		[1]		Black level offset value setting (4-wire)			
		[2]					
		[3]					
		[4]					
		[5]					
		[6]					
		[7]					
21h	3021h	[0]		MSB		00h	
		[1]		Fixed to “0”.	0h		—
		[2]		Fixed to “0”.	0h		—
		[3]		Fixed to “0”.	0h		—
		[4]	XHSLNG [1:0]	H sync pulse low level width setting 1.	0h		—
		[5]			0h		—
		[6]		Fixed to “0”.	0h		—
		[7]	10BITA	Setting registers for 10 bit.	0h		Immediately
22h	3022h	[0]	XVSLNG [2:0]	V sync pulse low level width setting.	0h	40h	Immediately
		[1]					
		[2]					
		[3]		Fixed to “0”.	0h		—
		[4]		Fixed to “0”.	0h		—
		[5]		Fixed to “0”.	0h		—
		[6]		Fixed to “1”.	1h		—
		[7]	720PMODE	Fixed to 1 for HD720p mode.	0h		V
23h to 26h	3023h to 3026h	[7:0] to [7:0]		Do not rewrite.	—	—	—
27h	3027h	[7:0]		Fixed to “20h”.*2	21h	21h	Immediately
28h to 2Bh	3028h to 302Bh	[7:0] to [7:0]		Do not rewrite.	—	—	—

Address		bit	Register name	Description	Default value after reset		Reflection timing
4-wire	I^{2}C				By register	By address	
2Ch	302Ch	[0]	XMSTA	Trigger for master mode operation start 0:Master mode operation start 1: Trigger standby	1h	01h	Immediately
		[1]		Fixed to “0”.	0h		—
		[2]		Fixed to “0”.	0h		—
		[3]		Fixed to “0”.	0h		—
		[4]		Fixed to “0”.	0h		—
		[5]		Fixed to “0”.	0h		—
		[6]		Fixed to “0”.	0h		—
		[7]		Fixed to “0”.	0h		—
2Dh	302Dh	[0]		Fixed to “0”.	0h	40h	—
		[1]	DCKDLY	DCK phase delay For SDR output ... 0: 0°, 1: 180° For DDR output... 0: 0°, 1: 90°	0h		V
		[2]		Fixed to “0”	0h		—
		[3]	BITSEL	10-bit output 2-bit shift 0: Left justified, 1: Right justified	0h		V
		[4]		Fixed to “0”.	0h		—
		[5]		Fixed to “0”.	0h		—
		[6]		Fixed to “1”.	1h		—
		[7]		Fixed to “0”.	0h		—
2Eh to 3Eh	302Eh to 303Eh	[7:0] to [7:0]		Do not rewrite.	—	—	—
3Fh	303Fh	[7:0]		Fixed to “0Ah”.*2	00h	00h	Immediately
40h to 4Eh	3040h to 304Eh	[7:0] to [7:0]		Do not rewrite.	—	—	—
4Fh	304Fh	[7:0]	SYNC2EN	Sync mode selection 07h: Normal sync mode 47h: DCK sync mode	07h	07h	Immediately
50h to 53h	3050h to 3053h	[7:0] to [7:0]		Do not rewrite.	—	—	—
54h	3054h	[0] [1] [2]	XHSLNG2	H sync pulse low level width setting 2.	0	00h	Immediately
		[3]		Fixed to “0”.	0		—
		[4]	SYNCSEL	Sync mode selection 0: Normal sync mode 1: DCK sync mode	0		Immediately
		[5]		Fixed to “0”.	0		—
		[6]		Fixed to “0”.	0		—
		[7]		Fixed to “0”.	0		—
55h to 79h	3055h to 3079h	[7:0] to [7:0]		Do not rewrite.	—	—	—

Address		bit	Register name	Description	Default value after reset		Reflection timing
4-wire	I²C				By register	By address	
7Ah	307Ah	[7:0]	10BITB	Setting registers for 10 bit.	00h	00h	Immediately
7Bh	307Bh	[7:0]	10BITC	Setting registers for 10 bit.	00h	00h	Immediately
7Ch to 97h	307Ch to 3097h	[7:0] to [7:0]		Do not rewrite.	—	—	—
98h	3098h	[0]	10B1080 P [11:0]	LSB Adjustment registers for each operation mode. MSB	226h	26h	Immediately
		[1]					
		[2]					
		[3]					
		[4]					
		[5]					
		[6]					
		[7]					
99h	3099h	[0]				02h	
		[1]					
		[2]					
		[3]					
		[4]		Fixed to “0”.	0h		—
		[5]		Fixed to “0”.	0h		—
		[6]		Fixed to “0”.	0h		—
		[7]		Fixed to “0”.	0h		—
9Ah	309Ah	[0]	12B1080 P [11:0]	LSB Adjustment registers for each operation mode. MSB	44Ch	4Ch	Immediately
		[1]					
		[2]					
		[3]					
		[4]					
		[5]					
		[6]					
		[7]					
9Bh	309Bh	[0]				04h	
		[1]					
		[2]					
		[3]					
		[4]		Fixed to “0”.	0h		—
		[5]		Fixed to “0”.	0h		—
		[6]		Fixed to “0”.	0h		—
		[7]		Fixed to “0”.	0h		—
9Ch to CDh	309Ch to 30CDh	[7:0] to [7:0]		Do not rewrite	—	—	—

Address 4-wire	Address I²C	bit	Register name	Description	Default value after reset By register	Default value after reset By address	Reflection timing
CEh	30CEh	[0]	PRES[6:0]	LSB	16h	16h	Immediately
		[1]					
		[2]					
		[3]		Adjustment registers for each operation mode.			
		[4]					
		[5]					
		[6]		MSB			
		[7]		Fixed to “0”.	0h		
CFh	30CFh	[0]	DRES[8:0]	LSB	082h	82h	Immediately
		[1]					
		[2]					
		[3]					
		[4]		Adjustment registers for each operation mode.			
		[5]					
		[6]					
		[7]					
D0h	30D0h	[0]		MSB		00h	
		[1]		Fixed to “0”.	0h		—
		[2]		Fixed to “0”.	0h		—
		[3]		Fixed to “0”.	0h		—
		[4]		Fixed to “0”.	0h		—
		[5]		Fixed to “0”.	0h		—
		[6]		Fixed to “0”.	0h		—
		[7]		Fixed to “0”.	0h		—
D1h to FFh	30D1h to 30FFh	[7:0] to [7:0]		Do not rewrite.	—	—	—

Chip ID: 03h

Address		Bit	Register name	Description	Default value after reset		Reflection timing
4-wire	I^2C				By register	By address	
00h to 16h	3100h to 3116h	[7:0] to [7:0]		Do not rewrite.	—	—	—
17h	3117h	[7:0]		Fixed to "0Dh" *2.	4Dh	4Dh	Immediately
18h to FFh	3118h to 31FFh	[7:0] to [7:0]		Do not rewrite.	—	—	—

*1 The STANDBY (Address 00h [0]) register is reflected at the following timings.
•When canceling standby mode: Reflected immediately
•When entering standby mode: Reflected immediately after the end of the frame during which the setting was made

*2 The values must be changed from the default values, so initial setting after reset is required after power-on. Subsequent setting by communication is not needed unless the power is turned Off or the system is reset.

*3 "V" in the "Reflection timing" column indicates that the setting value is reflected at the falling edge of the next XVS after the register communication is performed.

*4 Do not perform communication to addresses not listed in the Register Map. Doing so may result in malfunction. However, other registers that require communication to addresses not listed above may be added, so addresses up to FFh should be supported for both CID = 02h and 03h.

Readout Drive Mode

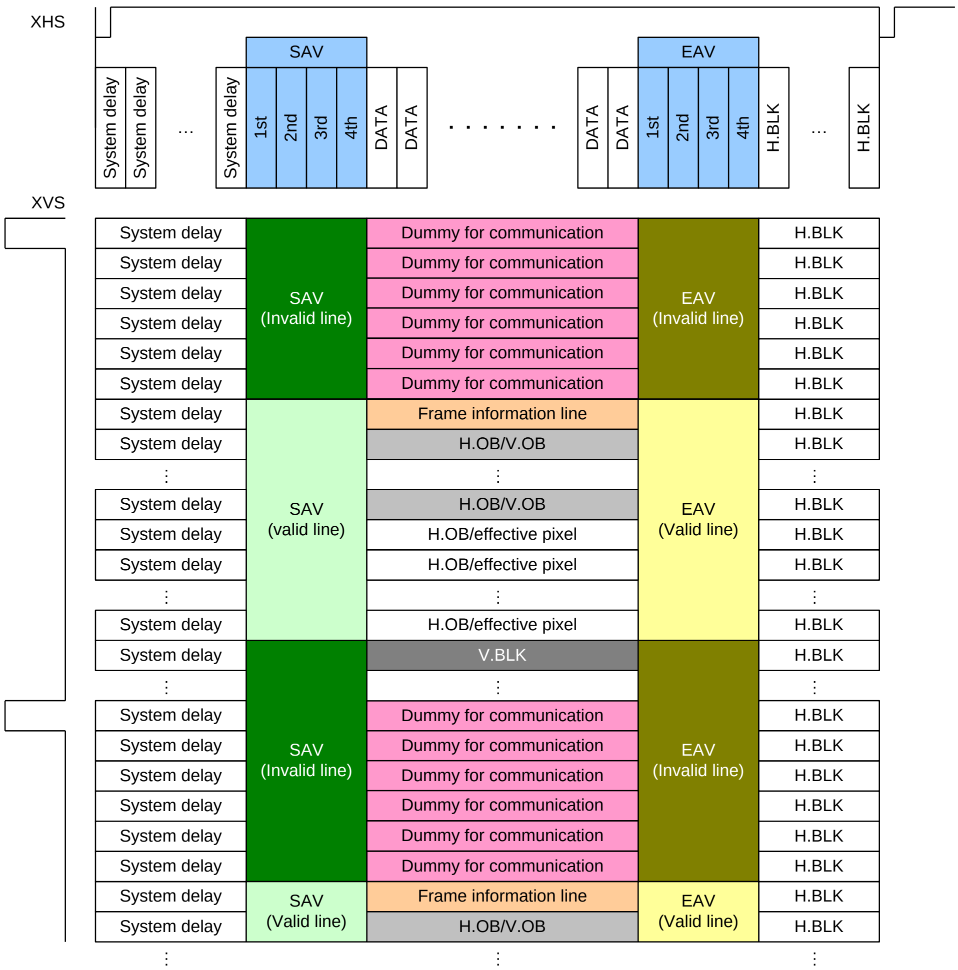
The table below lists the operating modes available with this sensor.

Drive mode	Imaging conditions								
	INCK [MHz]	Frame rate [frame/s]	Output Resolution [bit]	Data Rate [Mpixel/s]	Number of effective pixels		Data width*1		1H Period [µs]
					H [pixels]	V [lines]	H [INCK]	V [lines]	
HD1080 p	37.125	15.00	10/12	37.125	1984	1105	2200	1125	59.26
		25.00	10/12	74.25			1320		35.56
		30.00	10/12	74.25			1100		29.63
HD720 p		30.00	10/12	37.125	1344	745	1650	750	44.44
		60.00	10	74.25			825		22.22

*1 The data width indicates the output sync signal period in master mode. In slave mode the data width is the input XVS and XHS clock interval.

Sync Code

The sync code is added immediately before and after "dummy signal + OB signal + effective pixel data" and then output. The sync code is output in order of 1st, 2nd, 3rd and 4th. The fixed value is output for 1st to 3rd. (BLK: Blanking period)

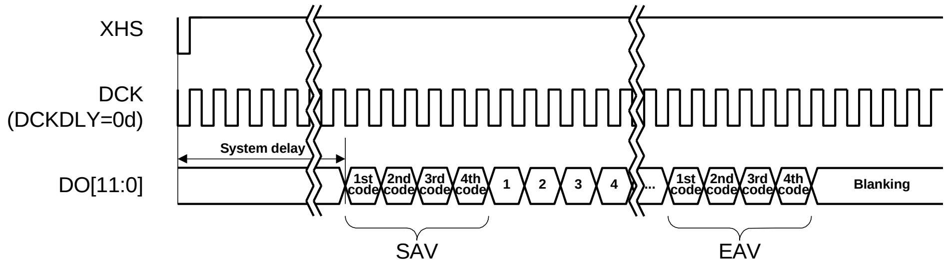


Sync code	1st code		2nd code		3rd code		4th code	
	10 bit	12 bit	10 bit	12 bit	10 bit	12 bit	10 bit	12 bit
SAV(Valid line)	3FFh	FFFh	000h	000h	000h	000h	200h	800h
EAV(Valid line)	3FFh	FFFh	000h	000h	000h	000h	274h	9D0h
SAV(Invalid line)	3FFh	FFFh	000h	000h	000h	000h	2ACh	AB0h
EAV(Invalid line)	3FFh	FFFh	000h	000h	000h	000h	2D8h	B60h

Sync Code Output Timing (Parallel CMOS Output)

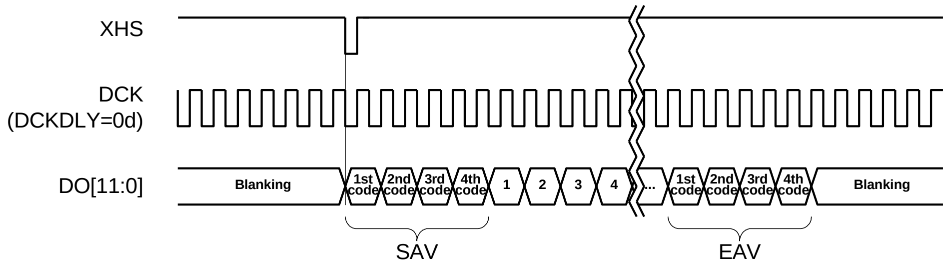
Sync Code Output Timing

In the normal sync mode, the sensor output signal passes through the internal circuits and is output with a latency time (system delay) relative to the horizontal sync signal. This system delay value is undefined for each line, so refer to the sync codes output from the sensor and perform synchronization.



Output Timing in Normal Sync Mode

The XVS and XHS fall timings can be changed as shown in figure below by setting to the DCK sync mode. In this time, the before the change XVS pulse can be output from TEST2 pin (F5 pin)



Output Timing in DCK sync Mode

Image Data Output Format

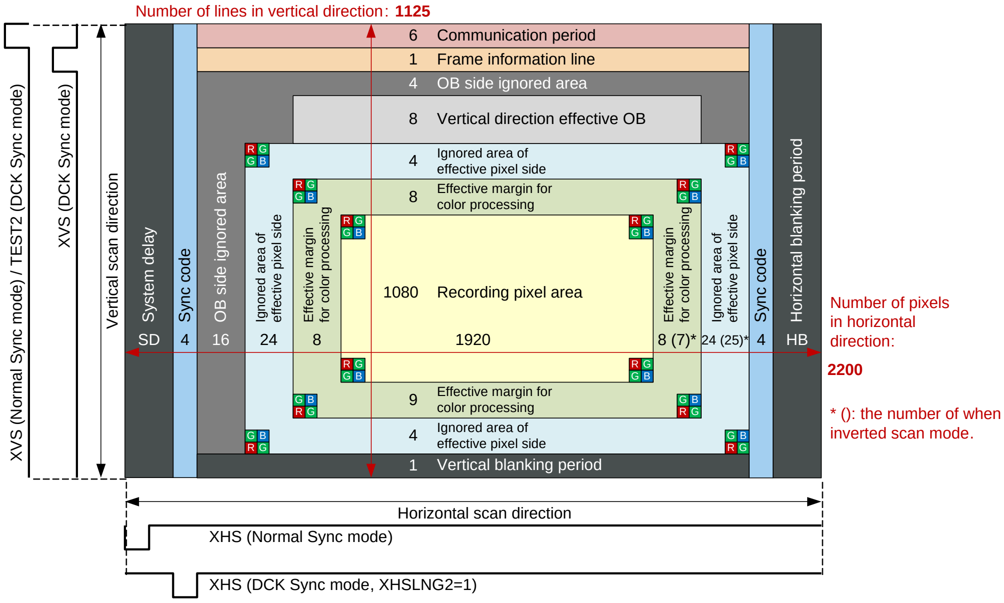
HD1080p Mode

The sensor signal is cut out with the angle of view for HD1080p (1920 × 1080) and read.

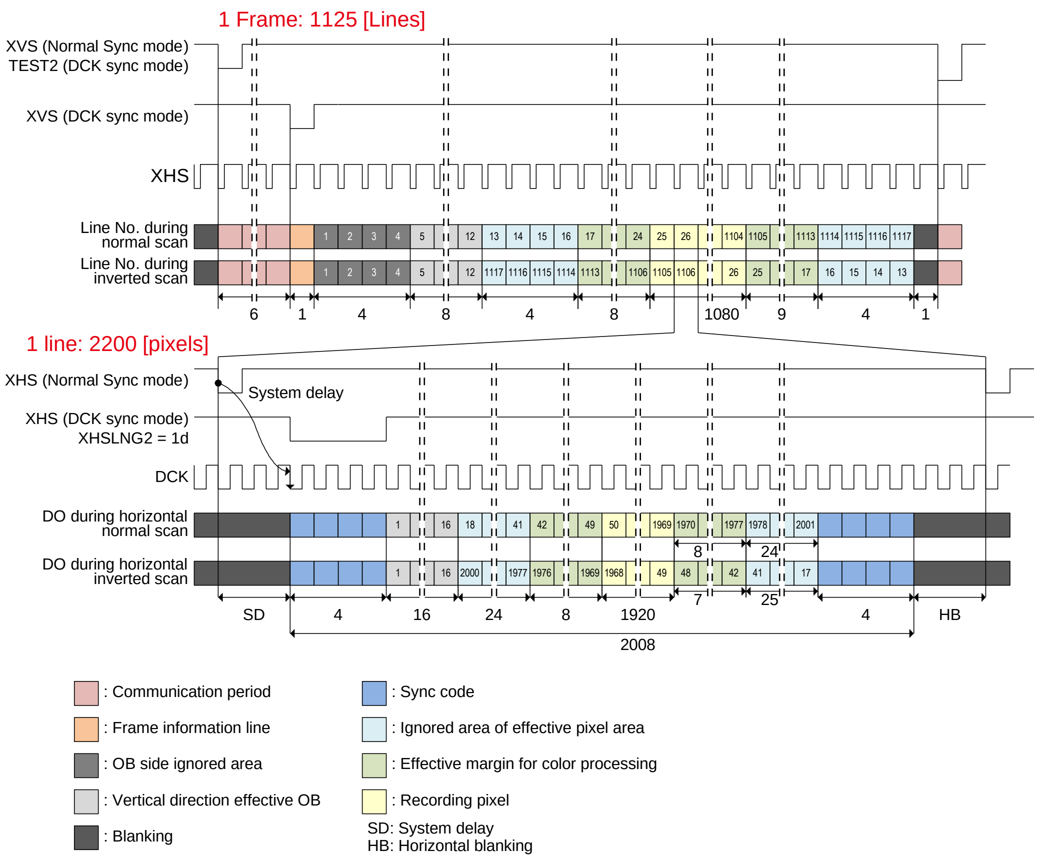
Register List for HD1080p Mode Setting

Register details			Initial value	Setting value				Function
Register name	Address	Bit		10 bit		12 bit		
				15 [frame/s]	30 [frame/s]	15 [frame/s]	30 [frame/s]	
I^2C ADRES1	0112h	[7:0]	0Ah	0Ah		0Ch		AD gradation setting (I^2C)
I^2C ADRES2	0113h	[7:0]	0Ah	0Ah		0Ch		AD gradation setting (I^2C)
FRM_ LENGTH	0340h	[7:0]	04E2h	0465h				Vertical (V) direction line number designation (I^2C)
	0341h	[7:0]						
LINE_ LENGTH	0342h	[7:0]	044Ch	0898h	044Ch	0898h	044Ch	Horizontal (H) direction clock number designation (I^2C)
	0343h	[7:0]						
MODE	02h	[3:0]	00h	Fh				HD1080 p mode
HMAX	03h	[7:0]	044Ch	0898h	044Ch	0898h	044Ch	Horizontal (H) direction clock number designation (4-wire)
	04h	[5:0]						
VMAX	05h	[7:0]	04E2h	0465h				Vertical (V) direction line number designation (4-wire)
	06h	[7:0]						
FRSEL	11h	[2:0]	0h	1h	0h	1h	0h	Output data rate designation
ADRES	12h	[1]	0h	0h		1h		AD gradation setting (4-wire)
WINPV	16h	[7:0]	00h	3Ch				Adjustments register for each operation mode
10BITA	21h	[7]	0	1		0		Adjustments register for each operation mode.
720PMODE	22h	[7]	0	0				Sets in 720 p mode only.
10BITB	7Ah	[7:0]	00h	40h		00h		Adjustments register for each operation mode.
10BITC	7Bh	[7:0]	00h	02h		00h		
10B1080 P	98h	[7:0]	226h	44Ch	226h			
	99h	[3:0]						
12B1080 P	9Ah	[7:0]	44Ch	44Ch			226h	
	9Bh	[3:0]						
PRES	CEh	[6:0]	16h	16h				
DRES	CFh	[7:0]	082h	082h				
	D0h	[0]						

Register details			Initial value	Setting value		Function
Register name	Address	Bit		10 bit	12 bit	
				25 [frame/s]		
I^2C ADRES1	0112h	[7:0]	0Ah	0Ah	0Ch	AD gradation setting (I^2C)
I^2C ADRES2	0113h	[7:0]	0Ah	0Ah	0Ch	AD gradation setting (I^2C)
FRM_ LENGTH	0340h	[7:0]	04E2h	0465h		Vertical (V) direction line number designation. (I^2C)
	0341h	[7:0]				
LINE_ LENGTH	0342h	[7:0]	044Ch	0528h		Horizontal (H) direction clock number designation. (I^2C)
	0343h	[7:0]				
MODE	02h	[3:0]	00h	Fh		HD1080p mode
HMAX	03h	[7:0]	044Ch	0528h		Horizontal (H) direction clock number designation. (4-wire)
	04h	[5:0]				
VMAX	05h	[7:0]	04E2h	0465h		Vertical (V) direction line number designation. (4-wire)
	06h	[7:0]				
FRSEL	11h	[2:0]	0h	0h		Output data rate designation.
ADRES	12h	[1]	0h	0h	1h	AD gradation setting. (4-wire)
WINPV	16h	[7:0]	00h	3Ch		Adjustments register for each operation mode.
10BITA	21h	[7]	0	1	0	Adjustments register for each operation mode.
720PMODE	22h	[7]	0	0		Sets in 720 p mode only.
10BITB	7Ah	[7:0]	00h	40h	00h	Adjustments register for each operation mode.
10BITC	7Bh	[7:0]	00h	02h	00h	
10B1080 P	98h	[7:0]	226h	294h	226h	
	99h	[3:0]				
12B1080 P	9Ah	[7:0]	44Ch	44Ch	294h	
	9Bh	[3:0]				
PRES	CEh	[6:0]	16h	16h		
DRES	CFh	[7:0]	082h	082h		
	D0h	[0]				



Pixel Array Image Drawing in HD1080p Mode



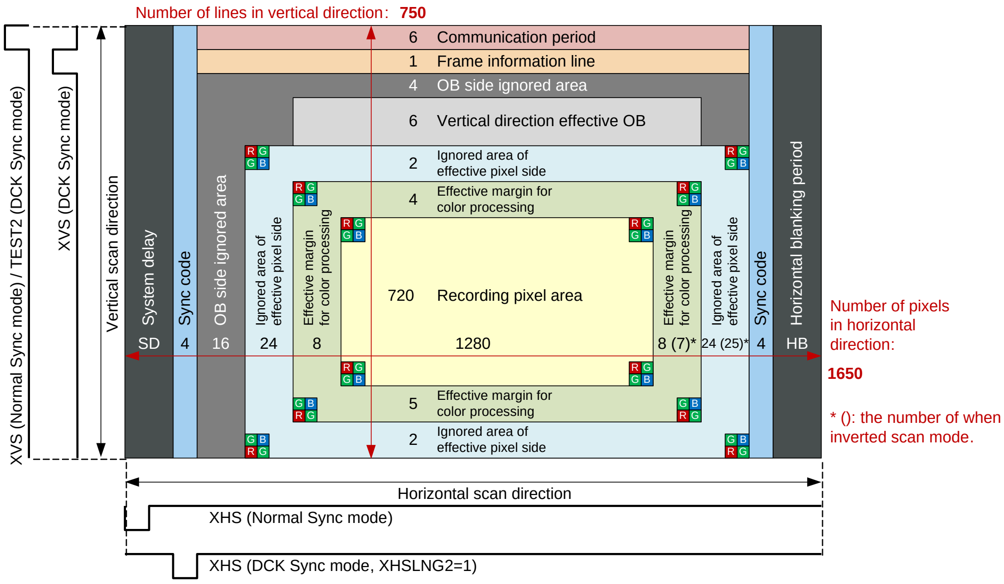
Drive Timing Chart in HD1080p Mode

HD720p mode

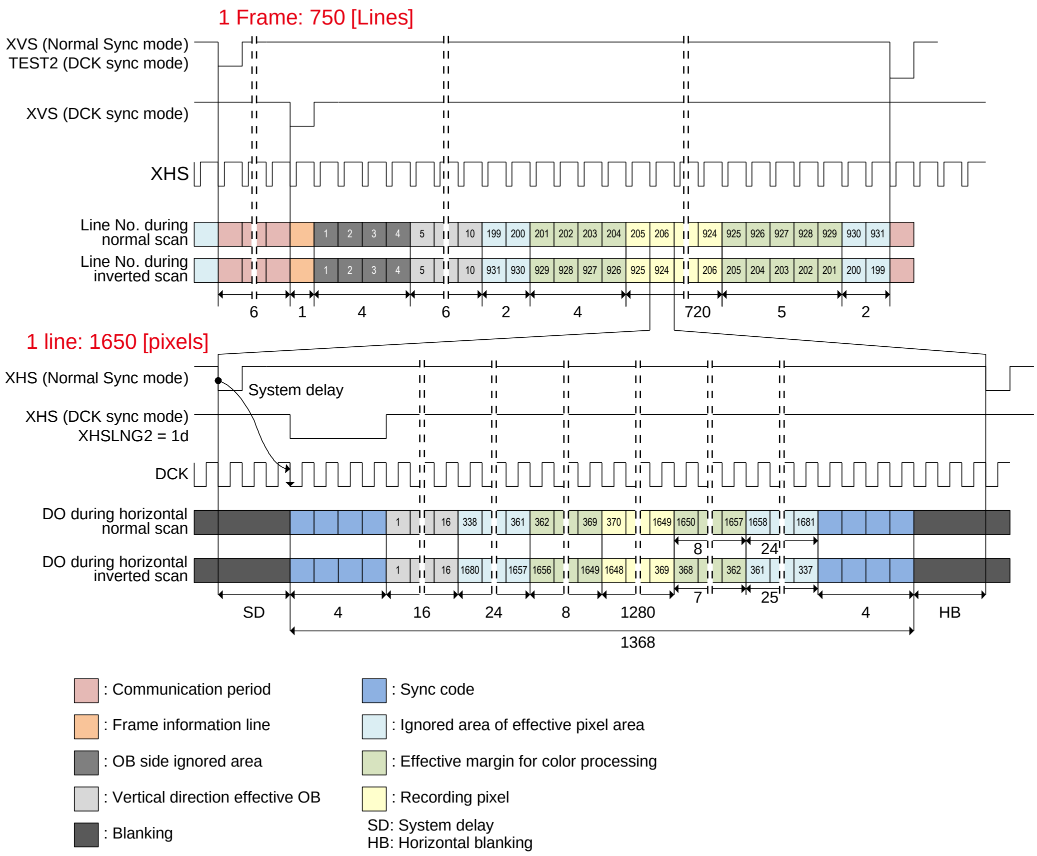
The sensor signal is cut out with the angle of view for HD720p (1280 × 720) and read.
However, set "1" to the register 720P MODE (Address 22h [7].)

Register List for HD720p Mode Setting

Register details: Register name	Address	Bit	Initial value	Setting value: 10 bit 30 [frame/s]	10 bit 60 [frame/s]	12 bit 30 [frame/s]	Function
I^{2}C ADRES1	0112h	[7:0]	0Ah	0Ah		0Ch	AD gradation setting. (I^{2}C)
I^{2}C ADRES2	0113h	[7:0]	0Ah	0Ah		0Ch	AD gradation setting. (I^{2}C)
FRM_ LENGTH	0340h	[7:0]	04E2h	02EEh			Vertical (V) direction line number designation. (I^{2}C)
	0341h	[7:0]					
LINE_ LENGTH	0342h	[7:0]	044Ch	0672h	0339h	0672h	Horizontal (H) direction clock number designation. (I^{2}C)
	0343h	[7:0]					
MODE	02h	[3:0]	0h	1h			HD720 p mode
HMAX	03h	[7:0]	044Ch	0672h	0339h	0672h	Horizontal (H) direction clock number designation. (4-wire)
	04h	[5:0]					
VMAX	05h	[7:0]	04E2h	02EEh			Vertical (V) direction line number designation. (4-wire)
	06h	[7:0]					
FRSEL	11h	[2:0]	0h	1h	0h	1h	Output data rate designation.
ADRES	12h	[1]	0h	0h		1h	AD gradation setting. (4-wire)
WINPV	16h	[7:0]	00h	F0h			Adjustments register for each operation mode.
10BITA	21h	[7]	0	1	0		Adjustments register for each operation mode.
720PMODE	22h	[7]	0	1			Sets in 720 p mode only.
10BITB	7Ah	[7:0]	00h	40h	00h		Adjustments register for each operation mode.
10BITC	7Bh	[7:0]	00h	02h	00h		
10B1080 P	98h	[7:0]	226h	226h			
	99h	[3:0]					
12B1080 P	9Ah	[7:0]	44Ch	44Ch			
	9Bh	[3:0]					
PRES	CEh	[6:0]	16h	00h		40h	
DRES	CFh	[7:0]	082h	000h		181h	
	D0h	[0]					



Pixel Array Image Drawing in HD720p Mode



Drive Timing Chart in HD720p Mode

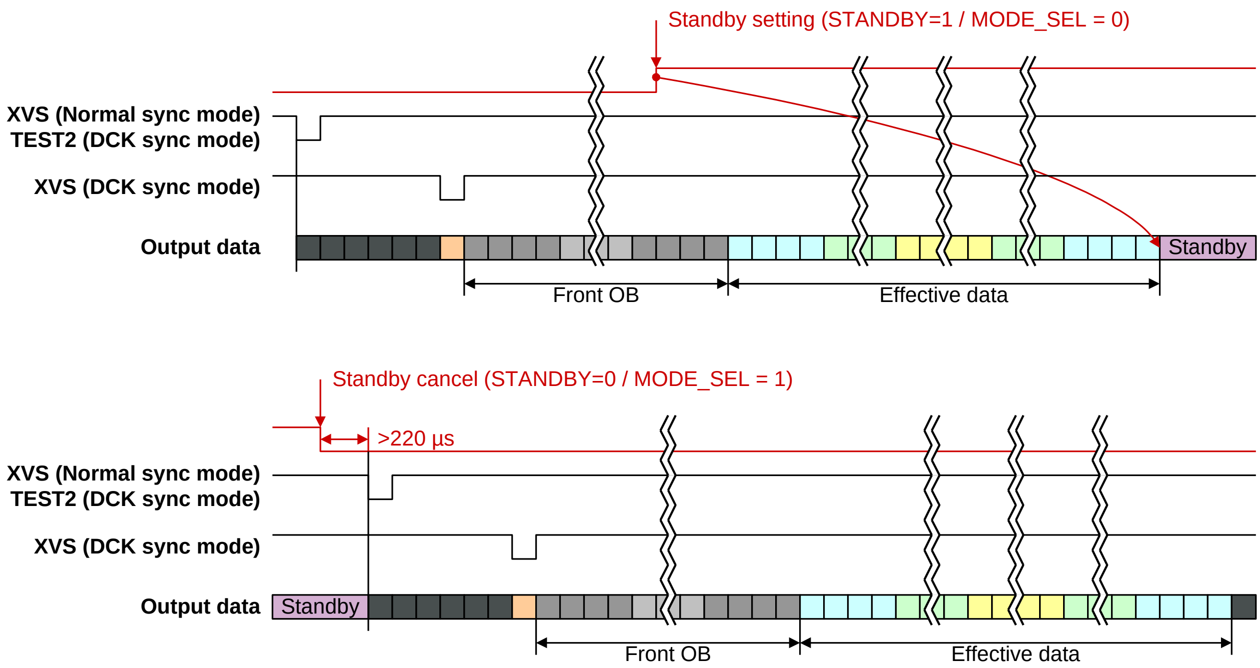
Description of Various Functions

Standby mode

This sensor stops its operation and goes into standby mode which reduces the power consumption by writing "1" to the standby control register STANDBY (address 00h, Bit [0]), in 4-wire communication, writing "0" to the register MODE_SEL (address 0100h, Bit [0]) (Standby mode immediately after power-on and reset).
Standby mode is reflected after V. OB after the set frame.
Write to register is possible because the serial communication function operates even in standby mode.
Set the STANDBY register to "0" to cancel standby mode. The standby cancel is immediately reflected from the communication.

List of Standby Mode Setting

Communication	Register details			Initial value	Setting value	Status		Remarks
	Register name	Address	Bit			Digital circuit	Analog circuit	
4-wire	STANDBY	00h	[0]	1	1 (Standby)	Stop	Stop	Register communication is executed even in standby mode.
					0	Operate	Operate	
I^2C	MODE_SEL	0100h	[0]	1	0 (Standby)	Stop	Stop	
					1	Operate	Operate	



Standby Mode Change Timing

Slave Mode and Master Mode

The sensor can be switched between slave mode and master mode. The switching is made by the XMASTER pin.
Set the XMSTA register (address 2Ch [0]) to “0” in order to start the operation after setting to master mode.
In addition, set the count number of sync signal in vertical direction by the VMAX register (address 05h [7:0], 06h [7:0]) (4-wire) / FRM_LENGTH register (address 0340h [7:0], 0341h [7:0]) (I^2C) and the clock number in horizontal direction by the HMAX register (address 03h [7:0], 04h [5:0]) (4-wire) / LINE_LENGTH register (address 0342h [7:0], 0343h [5:0]). See the description of Operation Mode for details of drive mode.

List of Slave and Master Mode Setting

Pin name	Pin processing	Operation mode	Remarks
XMASTER pin	Low fixed	Master Mode	High: 1.8 V Low: GND
	High fixed	Slave Mode	

Communication	Description of register			Initial value	Setting value	Status	Remarks
	Register name	Address (I^2C)	Bit			Master Mode	
4-wire / I^2C	XMSTA	2Ch (302Ch)	[0]	1h	0h	Master operation start	The master operation starts by setting to 0.
					1h	Master operation ready	
	XHSLNG	21h (3021h)	[5:4]	0h	See the diagram.		XHS width designated (In Normal sync mode)
	XVSLNG	22h (3022h)	[2:0]	0h			XVS width designated (In Normal sync mode) TEST2 width designated (In DCK sync mode)
	SYNC2EN	4Fh (304Fh)	[7:0]	07h	07h	Normal sync mode	Sync mode selection
					47h	DCK sync mode	
	XHSLNG2	54h (3054h)	[2:0]	0h	See the diagram		XHS width designated (In DCK sync mode)
	SYNCSEL		[4]	0h	0h	Normal sync mode	Sync mode selection
					1h	DCK sync mode	
4-wire	VMAX	05h	[7:0]	4E2h	See the each item in Operation Mode.		Line number per frame designated
		06h	[7:0]				
	HMAX	03h	[7:0]	44Ch			Clock number per frame designated
		04h	[5:0]				
I^2C	FRM_ LENGTH	0340h	[7:0]	04E2h	See the each item in Operation Mode.		Line number per frame designated
		0341h	[7:0]				
	LINE_ LENGTH	0342h	[7:0]	044Ch			Clock number per frame designated
		0343h	[7:0]				

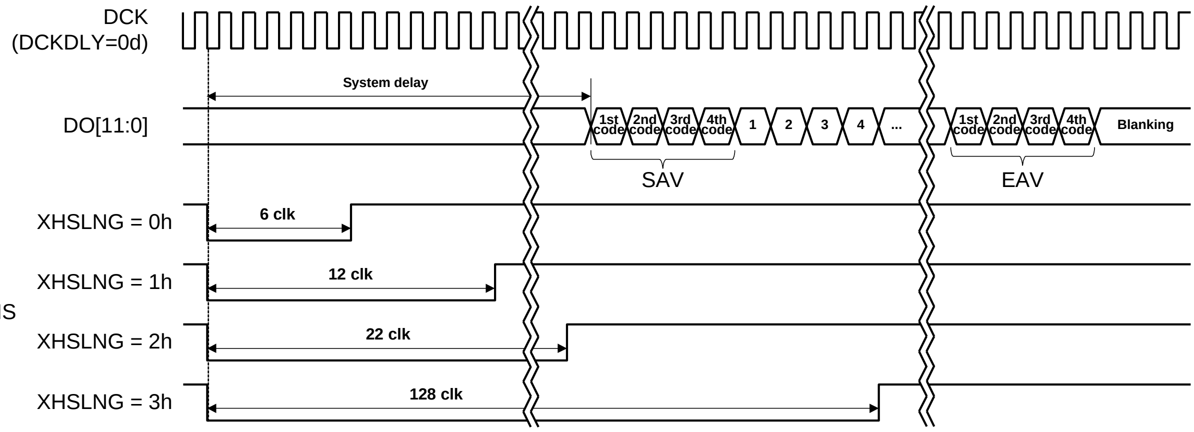
When a sensor is in slave mode, values set in the registers of the list above are invalid.

Normal Sync mode

The XVS and XHS are output in timing that set 0 to the register XMSTA. If set 0 to XMSTA during standby, the XVS and XHS are output just after standby is released. The XVS and XHS are output asynchronous with other input or output signals. In addition, the output signals are output with an undefined latency time (system delay) relative to the XHS. Therefore, refer to the sync codes output from the sensor and perform synchronization.

XHSLNG Selection

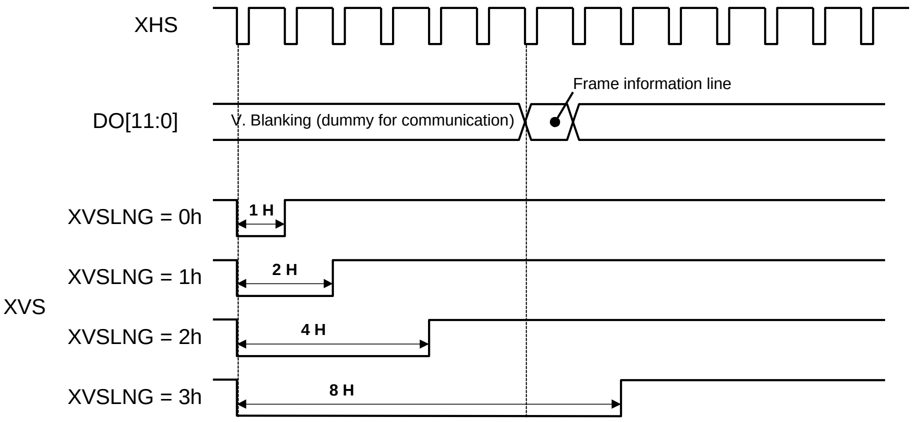
The low level pulse width of horizontal sync signal XHS is set by the XHSLNG register. The output has system delay from the XHS fall to effective data (sync code) output.



List of XHS Pulse Width Setting (Normal Sync mode)

XVSLNG Selection

The low level pulse width of vertical sync signal XVS is set.



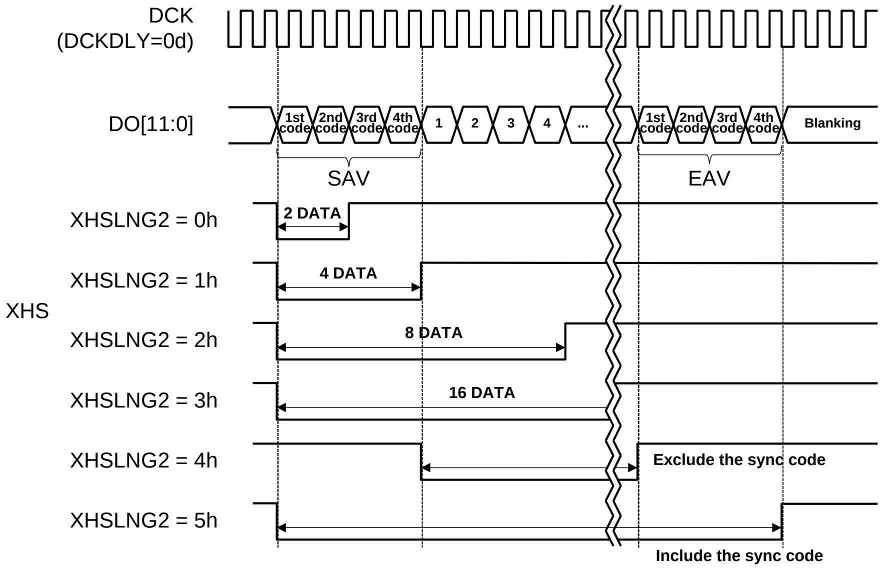
List of XVS Pulse Width Setting (Normal Sync mode)

DCK Sync mode

The DCK Sync mode is enabled by setting the register SYNC2EN (Address: 4Fh [7:0]) to 47h, register SYNCSEL (Address: 54h [4]) to 1h. In the DCK Sync mode, the XVS fall timing becomes the frame information line output timing, and the XHS fall timing becomes the sync code basis. The low level pulse width of XHS in the DCK Sync mode is designated by register XHSLNG2 (Address: 54h [2:0].) The communication timing is 6 H period after fall edge of TEST2 pulse. The low level pulse width of TEST2 is designated by register XVSLNG. On the other hand, the low level pulse width of XVS is fixed to 1 H period.

XHSLNG2 Selection

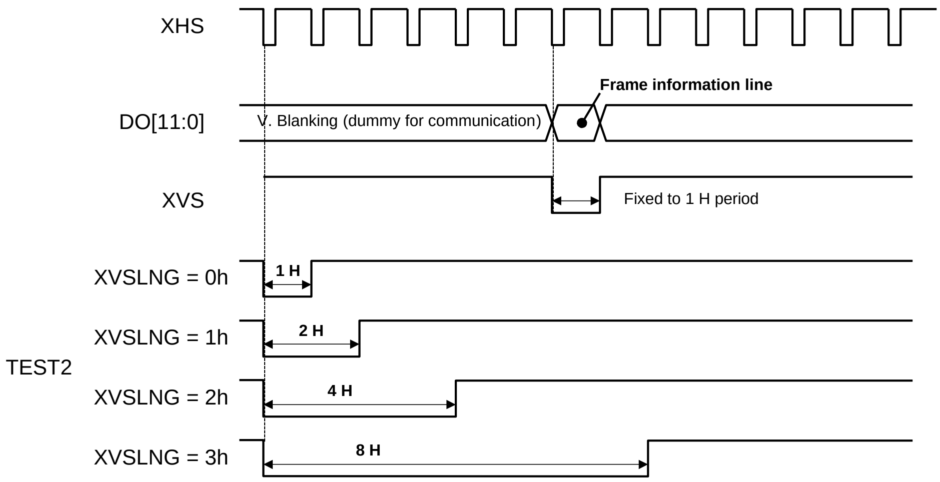
Set the low level pulse width of the XHS.



List of XHS Pulse Width Setting (DCK Sync mode)

XVSLNG Selection

Set the low level pulse width of the TEST2. The low level pulse width of the XVS is fixed to 1 H period.

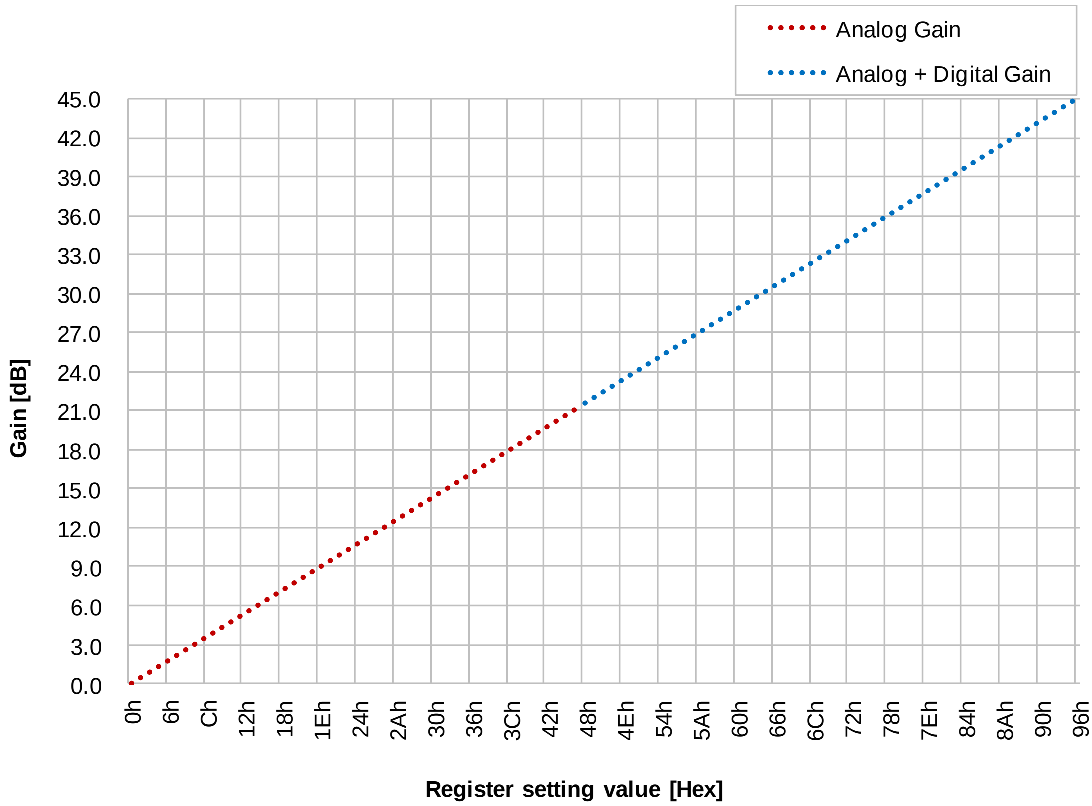


List of TEST2 Pulse Width Setting (DCK Sync mode)

Gain Adjustment Function

The Programmable Gain Control (PGC) of this device consists of the analog block and digital block.
The total of analog gain and digital gain can be set up to 45 dB by the GAIN register (address 1Eh [7:0]) setting.

See the List of Gain Setting Register Value for Each Register.



List of PGC Register

Register details			Initial value	Setting value		Remarks
Register name	Address (I^2C)	Bit		Min.	Max.	
GAIN	1Eh (301Eh)	[7:0]	00h	00h	96h	See the next page.

List of Gain Setting Register Value

Gain [dB]	GAIN [7:0]	Gain [dB]	GAIN [7:0]	Gain [dB]	GAIN [7:0]
0.0	0h	15.3	33h	30.6	66h
0.3	1h	15.6	34h	30.9	67h
0.6	2h	15.9	35h	31.2	68h
0.9	3h	16.2	36h	31.5	69h
1.2	4h	16.5	37h	31.8	6Ah
1.5	5h	16.8	38h	32.1	6Bh
1.8	6h	17.1	39h	32.4	6Ch
2.1	7h	17.4	3Ah	32.7	6Dh
2.4	8h	17.7	3Bh	33.0	6Eh
2.7	9h	18.0	3Ch	33.3	6Fh
3.0	Ah	18.3	3Dh	33.6	70h
3.3	Bh	18.6	3Eh	33.9	71h
3.6	Ch	18.9	3Fh	34.2	72h
3.9	Dh	19.2	40h	34.5	73h
4.2	Eh	19.5	41h	34.8	74h
4.5	Fh	19.8	42h	35.1	75h
4.8	10h	20.1	43h	35.4	76h
5.1	11h	20.4	44h	35.7	77h
5.4	12h	20.7	45h	36.0	78h
5.7	13h	21.0	46h	36.3	79h
6.0	14h	21.3	47h	36.6	7Ah
6.3	15h	21.6	48h	36.9	7Bh
6.6	16h	21.9	49h	37.2	7Ch
6.9	17h	22.2	4Ah	37.5	7Dh
7.2	18h	22.5	4Bh	37.8	7Eh
7.5	19h	22.8	4Ch	38.1	7Fh
7.8	1Ah	23.1	4Dh	38.4	80h
8.1	1Bh	23.4	4Eh	38.7	81h
8.4	1Ch	23.7	4Fh	39.0	82h
8.7	1Dh	24.0	50h	39.3	83h
9.0	1Eh	24.3	51h	39.6	84h
9.3	1Fh	24.6	52h	39.9	85h
9.6	20h	24.9	53h	40.2	86h
9.9	21h	25.2	54h	40.5	87h
10.2	22h	25.5	55h	40.8	88h
10.5	23h	25.8	56h	41.1	89h
10.8	24h	26.1	57h	41.4	8Ah
11.1	25h	26.4	58h	41.7	8Bh
11.4	26h	26.7	59h	42.0	8Ch
11.7	27h	27.0	5Ah	42.3	8Dh
12.0	28h	27.3	5Bh	42.6	8Eh
12.3	29h	27.6	5Ch	42.9	8Fh
12.6	2Ah	27.9	5Dh	43.2	90h
12.9	2Bh	28.2	5Eh	43.5	91h
13.2	2Ch	28.5	5Fh	43.8	92h
13.5	2Dh	28.8	60h	44.1	93h
13.8	2Eh	29.1	61h	44.4	94h
14.1	2Fh	29.4	62h	44.7	95h
14.4	30h	29.7	63h	45.0	96h
14.7	31h	30.0	64h		
15.0	32h	30.3	65h		

Black Level Adjustment Function

The black level offset (offset variable range: 03Ch to 1FFh) can be added relative to the data in which the digital gain modulation was performed by the BLKLEVEL register (address: 20h [7:0], 21h [0]) or I^2CBLKLEVEL register (address: 0008h [0], 0009 [7:0]). When the BLKLEVEL setting is increased by 1 LSB, the black level is increased by 1 LSB.

Use with values shown below is recommended.
10-bit output: 3Ch (60d)
12-bit output: F0h (240d)

List of Black Level Adjustment Register

Communication	Register details			Initial value	Setting value	
	Register name	Address	Bit		Min.	Max.
4-wire	BLKLEVEL	20h	[7:0]	03Ch	03Ch	1FFh
		21h	[0]			
I^2C	I^2C BLKLEVEL	0008h	[0]	040h	03Ch	1FFh
		0009h	[7:0]			

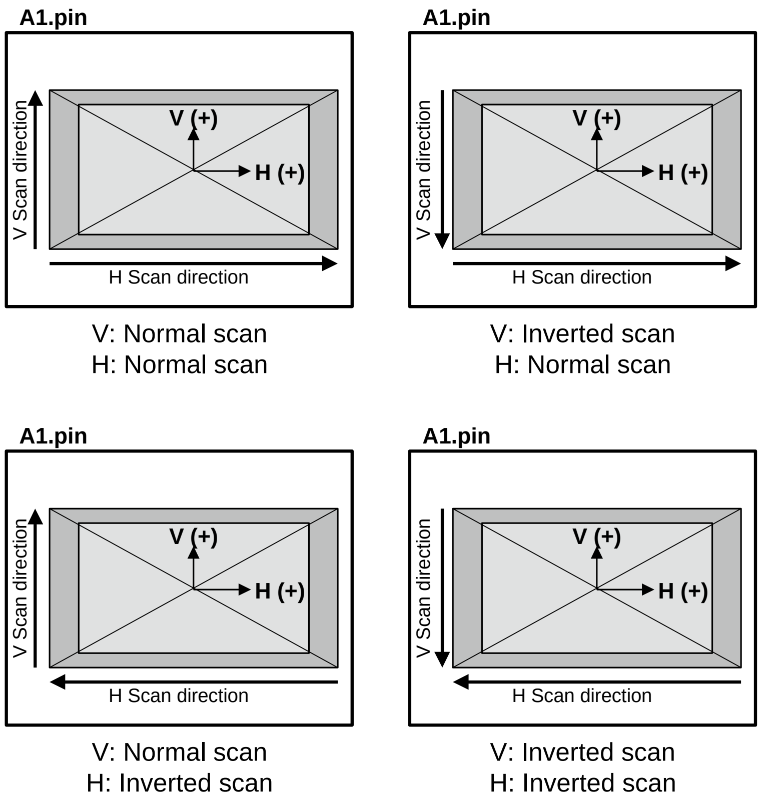
Horizontal and Vertical - Normal and Inverted Scan

The sensor readout direction (normal / inverted) in horizontal direction can be switched by the register HREVERSE (address: 01h [1]) in 4-wire, the register IMG_ORIENTATION_H (address: 0101h [0]) in I^2C.

The sensor readout direction (normal/inverted) in vertical direction can be switched by the VREVERSE (address 01h [0]) / IMG_ORIENTATION (address 0101h [1]) register setting. See the item of “Drive mode” for the order of readout lines in normal and inverted modes. One invalid frame is generated when reading immediately after the readout direction change in order to switch the normal operation and inversion between frames.

List of Vertical Drive Direction Setting Register

Communication	Register details			Initial value	Setting value	
	Register name	Address	Bit		Normal	Inverted
4-wire	VREVERSE	01h	[0]	0	0 (Vertical)	1 (Vertical)
	HREVERSE		[1]	0	0 (Horizontal)	1 (Horizontal)
I^2C	IMG_ORIENTATION_H	0101h	[0]	0	0 (Horizontal)	1 (Horizontal)
	IMG_ORIENTATION_V		[1]	0	0 (Vertical)	1 (Vertical)



Normal and Inverted Drive Outline

Shutter and Integration Time Settings

This sensor has a variable electronic shutter function that can control the integration time in line units. In addition, this sensor performs rolling shutter operation in which electronic shutter and readout operation are performed sequentially for each line.

Note) For integration time control, an image which reflects the setting is output from the frame after the setting changes.

Example of Integration Time Setting

The sensor's integration time is obtained by the following formula.

Integration time = 1 frame period - (SHS1) × (1H period) - 0.3 [H]

Note) 1. The frame period is determined by the input XVS when the sensor is operating in slave mode, or the register VMAX value in master mode. The frame period is designated in 1H units, so the time is determined by (Number of lines × 1H period).
2. See “Drive Modes” for the 1H period.

In this item, the shutter operation and integration time are shown as in the figure below with the time sequence on the horizontal axis and the vertical address on the vertical axis. For simplification, shutter and readout operation are noted in line units.

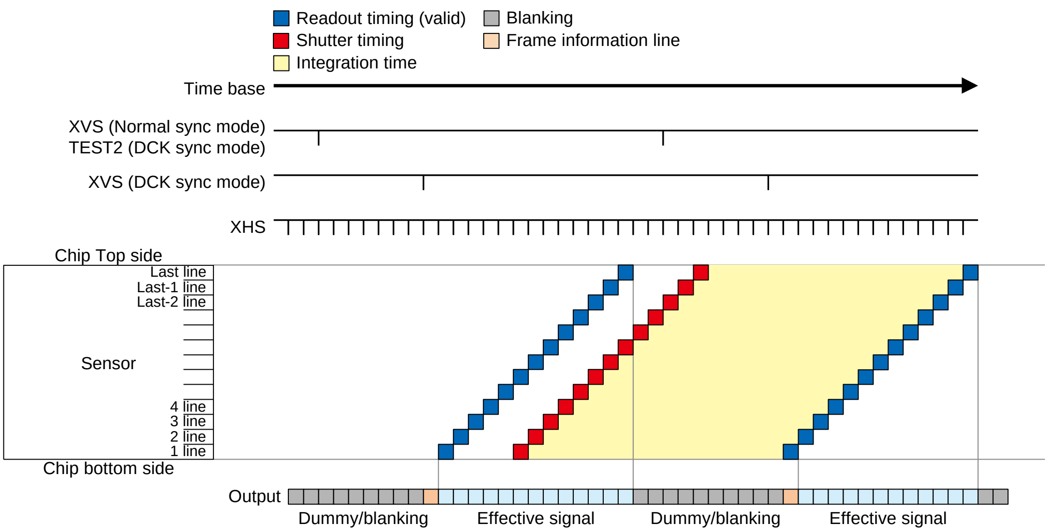


Image Drawing of Shutter Operation

Normal Exposure Operation (Controlling the Integration Time in 1H Units)

The integration time can be controlled by varying the electronic shutter timing. In the electronic shutter settings, the integration time is controlled by the SHS1 register (address: 08h [7:0], 09h [7:0]) (4-wire) / INTEG_TIME register (address: 0202h [7:0], 0203h [7:0]) (I^2C).
Set SHS1/INTEG_TIME to a value between 0 and (Number of lines per frame - 1). When the sensor is operating in slave mode, the number of lines per frame is determined by the XVS interval (number of lines), using the input XHS interval as the line unit. When the sensor is operating in master mode, the number of lines per frame is determined by the VMAX register (address: 05h [7:0], 06h [7:0]) (4-wire) / FRM_LENGTH register (address: 0340h [7:0], 0341h [7:0]) (I^2C). The number of lines per frame varies according to the drive mode.

Registers Used to Set the Integration Time in 1H Units

Communication	Register details			Initial value	Description
	Register name	Address	Bit		
4-wire	SHS1	08h	[7:0]	0000h	Sets the shutter sweep time.
		09h	[7:0]		
	VMAX	05h	[7:0]	04E2h	Sets the number of lines per frame (only in master mode). See "Operating Modes" for the setting value in each mode.
		06h	[7:0]		
I^2C	INTEG_TIME	0202h	[7:0]	0000h	Sets the shutter sweep time.
		0203h	[7:0]		
	FRM_LENGTH	0340h	[7:0]	04E2h	Sets the number of lines per frame (only in master mode). See "Operating Modes" for the setting value in each mode.
		0341h	[7:0]		

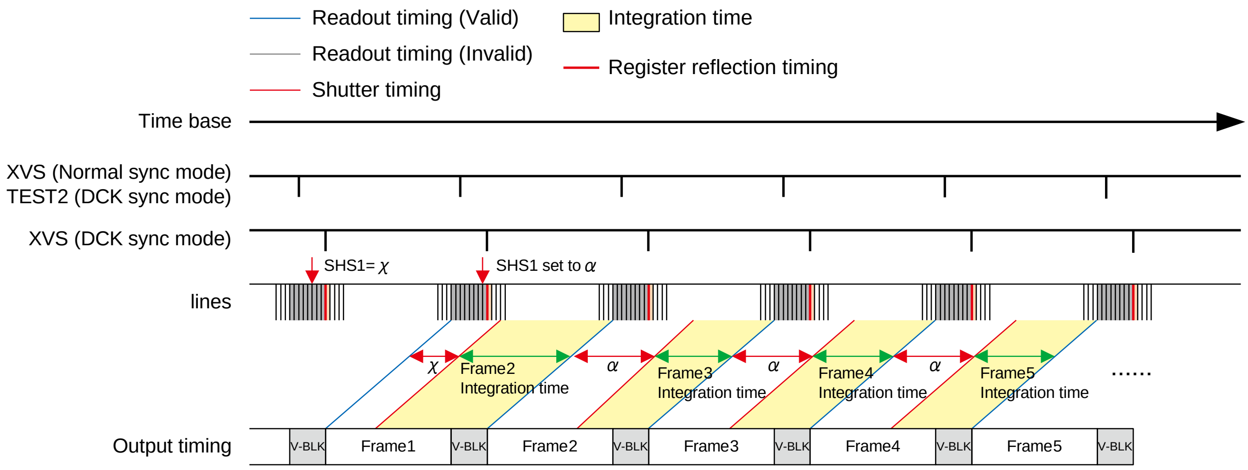


Image Drawing of Integration Time Control within a Frame

Long Exposure Operation (Control by Expanding the Number of Lines per Frame)

Long exposure operation can be performed by lengthening the frame period.
When the sensor is operating in slave mode, this is done by lengthening the input vertical sync signal (XVS) pulse interval. When the sensor is operating in master mode, it is done by designating a larger register VMAX (address: 05h [7:0], 06h [7:0]) value compared to normal operation.
Likewise, in slave mode the integration time can be increased by lengthening the input XVS signal pulse interval.
When the integration time is extended by increasing the number of lines, the rear V blanking increases by an equivalent amount.

The maximum VMAX and SHS1 values are 65535d. When the number of lines per frame is set to the maximum value, the integration time in HD1080p mode at 30 frame/s is approximately 1.9 s. When set to a number of V lines or more than that noted for each readout drive mode, the imaging characteristics are not guaranteed during long exposure operation.

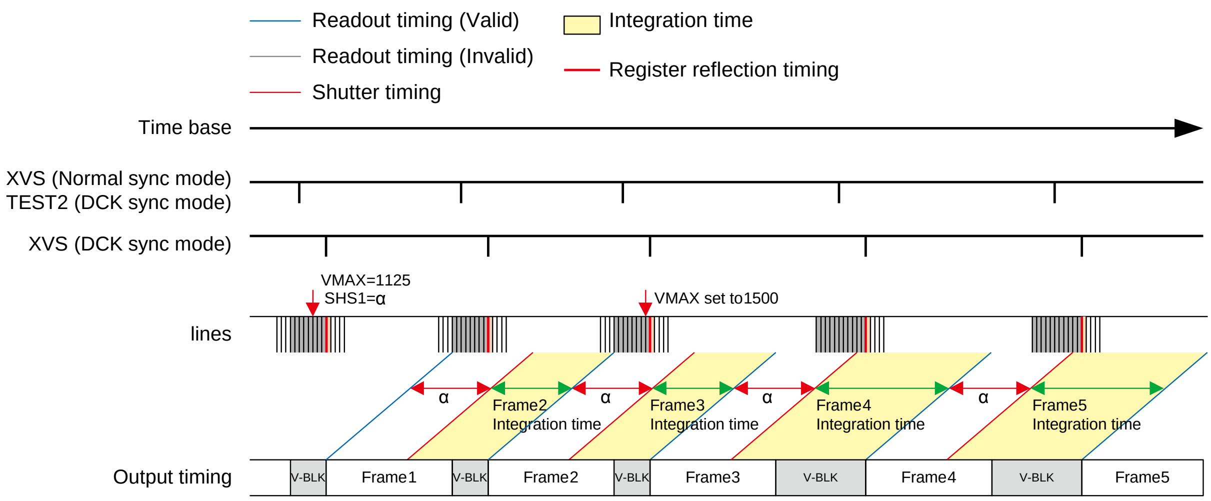


Image Drawing of Long Exposure Time Control by Adjusting the Frame Period

Example of Integration Time Setting

The example of register setting for controlling the integration time is shown below.

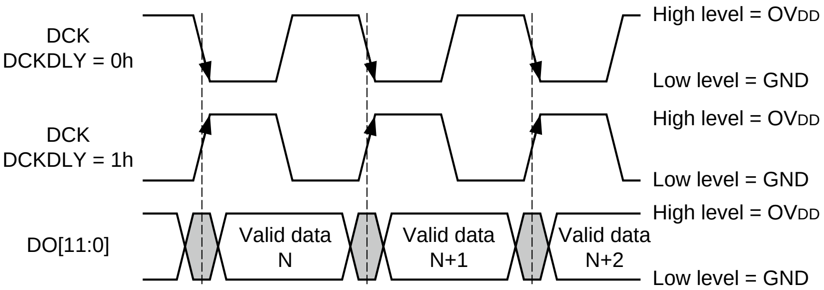
Example of Integration Time Setting (in HD1080p mode)

Operation	Sensor setting (Register)		Integration time
	VMAX*	SHS1 / INTEG_TIME	
Normal frame rate	1125	1124	0.7H period
		1123	1.7H period
		:	:
		N	(1125 – N – 0.3) H period
		:	:
		1	1123.7H period
		0	1124.7H period
Long-time exposure operation (control by expanding the number of lines per frame)	1126	0	1125.7H period
	1127	0	1126.7H period
	:	:	:
	M	N	(M – N – 0.3) H period
	:	:	:

* In sensor master mode. XVS interval to be input in slave mode.
* The SHS1 or the INTEG_TIME setting value (N) are set to the VMAX value (M) of -7 to 0.

Output Signal Interface Control

This sensor supports the following output formats. See “Image Data Output Format” for the data rate. Shaded areas in the figure indicate invalid data with regards to the AC characteristics. See “AC Characteristics” for details.



Example of Pin Waveform in CMOS 1-port SDR Output Mode

The sensor signal is output in sync with the falling edge of the data clock (DCK). (When DCKDLY is set to “0h”) Output in sync with the rising edge is possible by setting DCKDLY to “1h”.

Output Formats and Setting Methods

Communication	Register details			Initial value	Description
	Register name	Address (I^2C)	Bit		
4-wire	ADRES	12h	[1]	0	0: 10-bit output, 1: 12-bit output
I^2C	I^2C ADRES1	0112h	[7:0]	0Ah	0Ah: 10-bit output, 0Ch: 12-bit output
	I^2C ADRES2	0113h	[7:0]	0Ah	0Ah: 10-bit output, 0Ch: 12-bit output
4-wire/I^2C	DCKDLY	2Dh (302Dh)	[1]	0	Output in sync with the 0: falling edge, 1:rising edge.

Output Signal Range

The output gradation of this sensor can be switched to 10 bits or 12 bits. In parallel CMOS output mode, the output 10 bits or 12 bits are assigned to 10 pins or 12 pins, respectively. When set to 10 bits, the data is output from DO11 to DO2, and the unused pins are fixed Low.

Bit Assignment for Each Output Gradation

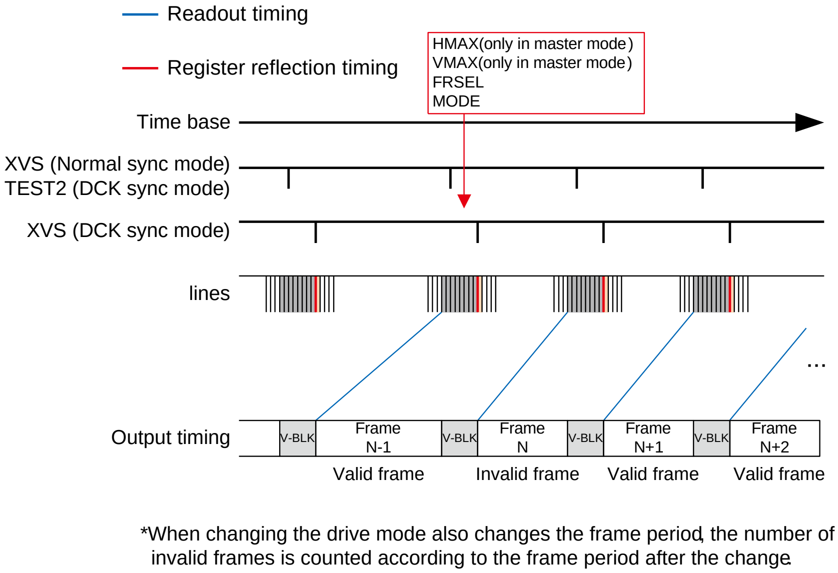
DO pin	Output bit assignment	
	10 bit	12 bit
DO [11]	DO [9]	DO [11]
DO [10]	DO [8]	DO [10]
DO [9]	DO [7]	DO [9]
DO [8]	DO [6]	DO [8]
DO [7]	DO [5]	DO [7]
DO [6]	DO [4]	DO [6]
DO [5]	DO [3]	DO [5]
DO [4]	DO [2]	DO [4]
DO [3]	DO [1]	DO [3]
DO [2]	DO [0]	DO [2]
DO [1]	Fixed to “0”	DO [1]
DO [0]	Fixed to “0”	DO [0]

Output Range

Output gradation	Output range	
	Minimum value	Maximum value
10 bit	000h	3FEh
12 bit	000h	FFEh

Mode Transitions

When changing the drive mode during sensor drive operation, an invalid frame is output. Data is output from sensor during the invalid frame period, but the output values may not reflect the integration time or may not be uniform on the screen, or a partially saturated image may be output.



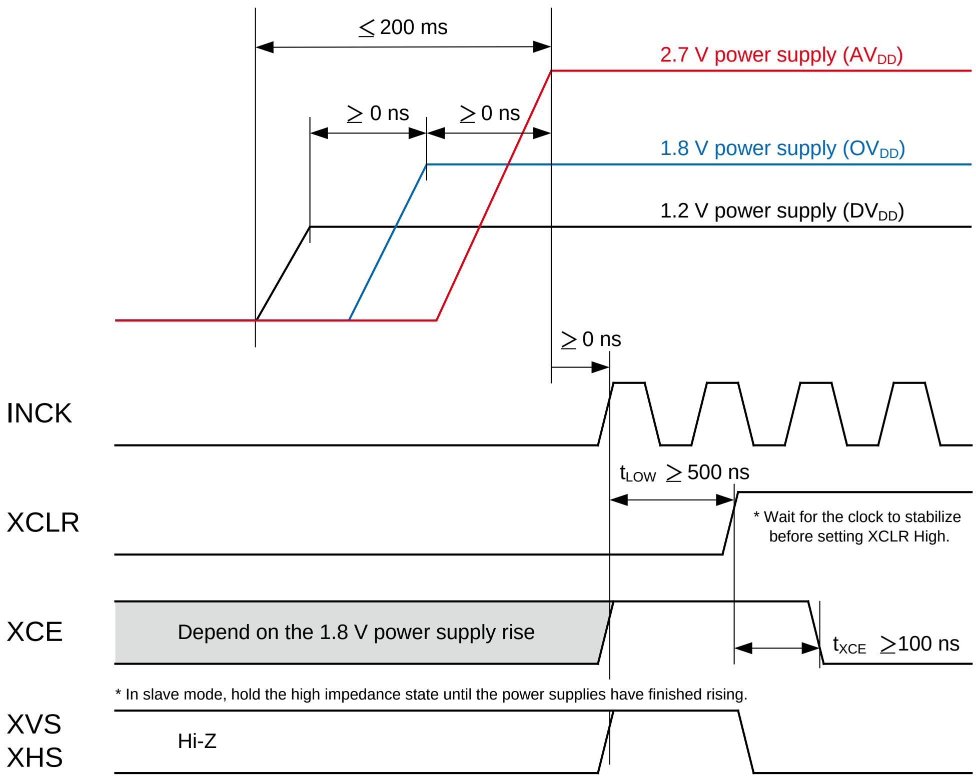
Invalid Frame Generation Timing

Power-on/off Sequence

Power-on Sequence

Follow the sequence below to turn on the power supplies.

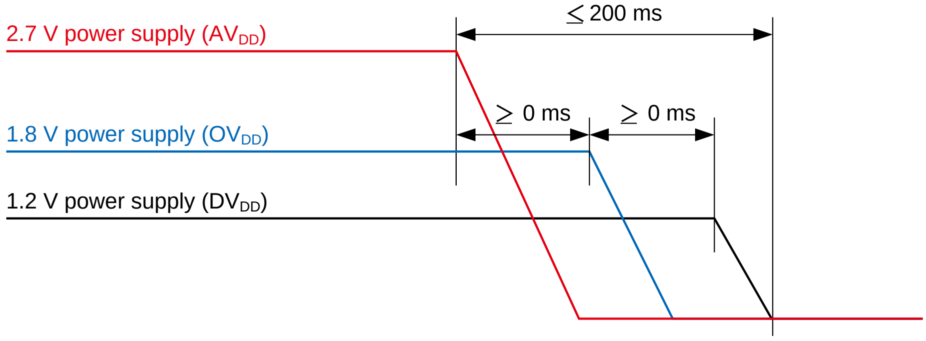
1. Turn on the power supplies so that the power supplies rise in order of 1.2 V power supply (DV_{DD}) → 1.8 V power supply (OV_{DD}) → 2.7 V power supply (AV_{DD}). In addition, all power supplies should finish rising within 200 ms.
2. Start master clock (INCK) input after turning on the power supplies.
3. The register values are undefined immediately after power-on, so the system must be cleared. Hold XCLR at Low level for 500 ns or more after all the power supplies have finished rising. (The register values after a system clear are the default values.)
   In addition, hold XCE at High level during this period. The XCE rise timing differs according to the 1.8 V power supply (OV_{DD}), so hold XCE at High level until INCK is input.
   The system clear is applied by setting XCLR to High level. However, the master clock needs to stabilize before setting the XCLR pin to High level.
4. Make the sensor settings by register communication after the system clear. A period of 100 ns or more should be provided after setting XCLR High before inputting the communication enable signal XCE in 4-wire communication.



Power-on Sequence

Power-off Sequence

Turn Off the power supplies so that the power supplies fall in order of 2.7 V power supply (AV_{DD}) → 1.8 V power supply (OV_{DD}) → 1.2 V power supply (DV_{DD}). In addition, all power supplies should finish falling within 200 ms. Set each digital input pin (INCK, XCE, SCK, SDI, XCLR, XMASTER, XVS, XHS) to 0 V or high impedance before the 1.8 V power supply (OV_{DD}) falls.



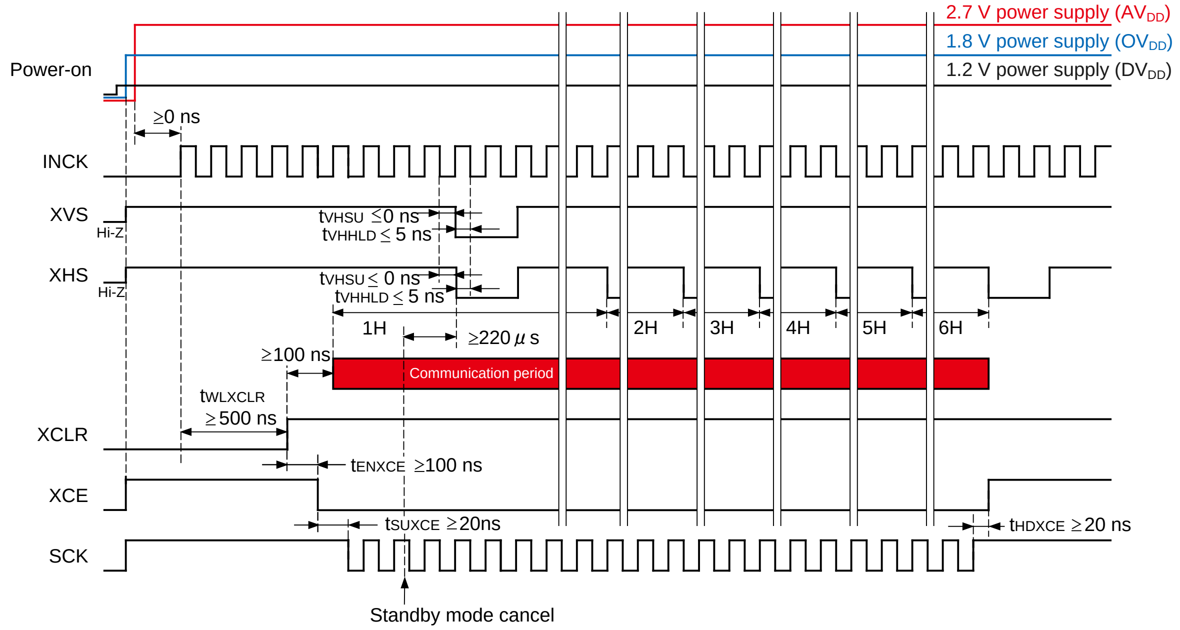
Power-off Sequence

Serial Communication Period after Sensor Reset

Slave mode

The communication period is set at the timing shown below for the sensor initial settings immediately after power-on. In slave mode, the vertical and horizontal sync signals (XVS, XHS) become valid only from the falling edges 100 ns or more after sensor reset (after XCLR is set Low). The 6H serial communication period is from the falling edge of the first valid XVS to the sixth XHS falling edge thereafter.

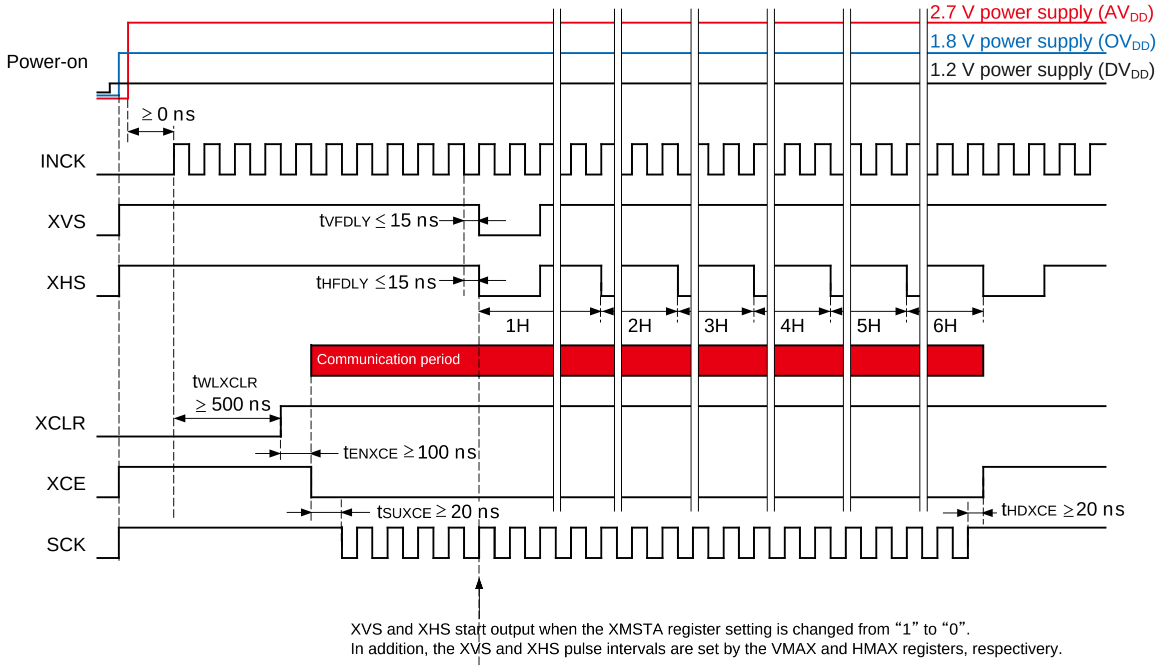
Note) XVS and XHS signals input when XCLR is Low are ignored. At this time the sensor is in standby mode until the next XVS signal. Register communication is possible in standby mode.



Communication Period after Sensor Reset in Slave Mode

Master mode

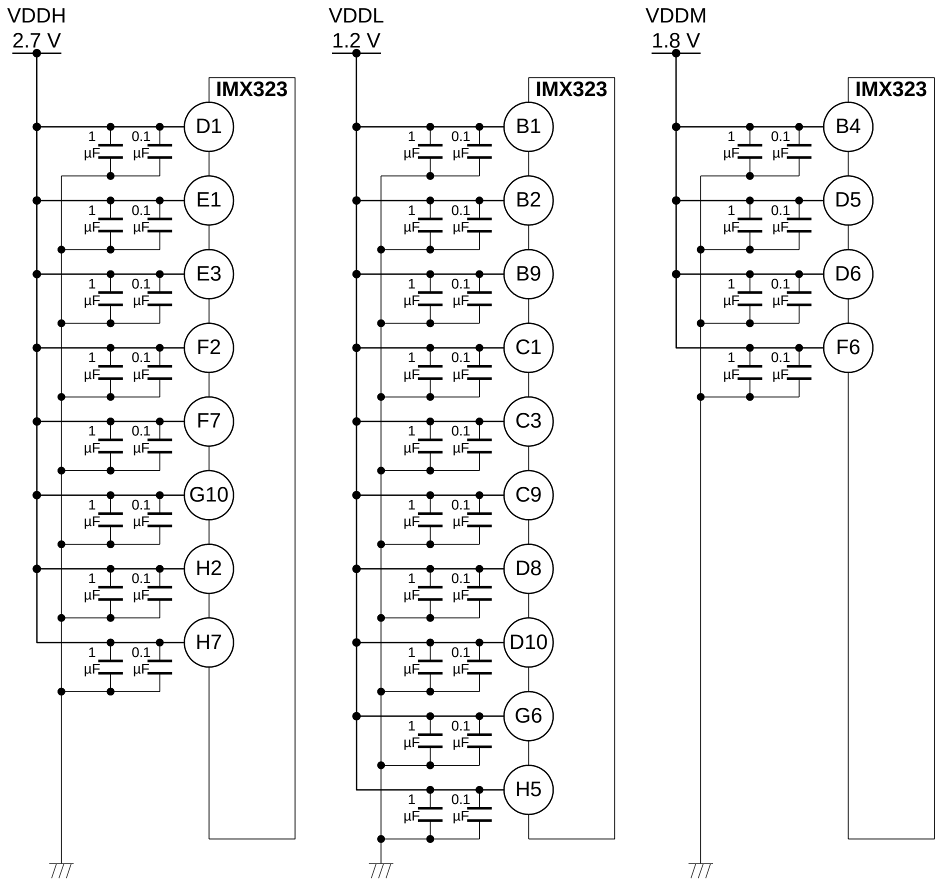
In master mode, the HMAX register (address 03h [7:0], 04h [5:0]) initial value is “44Ch” and the VMAX register (address 05h [7:0], 06h [7:0]) initial value is “4E2h”, so both XVS and XHS are output at these initial setting V and H widths until the setting values are reflected 6H later. When the VMAX and HMAX registers are set to arbitrary values by serial communication at the initial setting, and the master mode start register XMSTA (address 2Ch [0]) setting is changed from “1” to “0”, XVS and XHS start output according to the set values from the 7th H after the register settings are reflected. However, when VMAX and HMAX are set during the standby period, XVS and XHS are output according to the set values after standby is canceled.



Communication Period after Sensor Reset in Master Mode

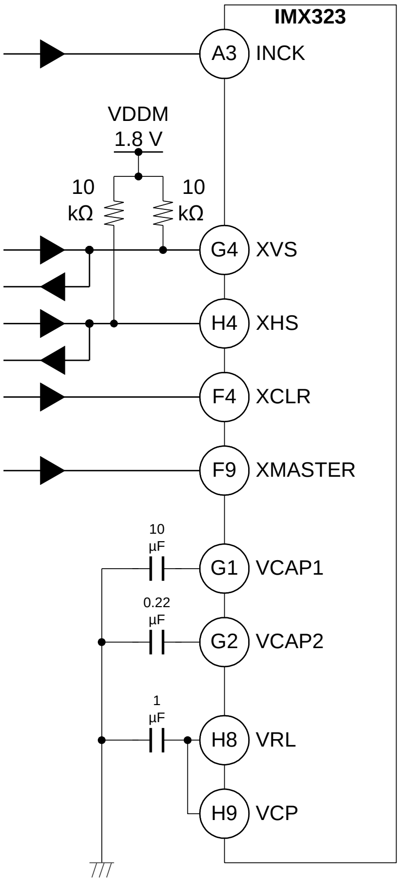
Peripheral Circuit

Power pins

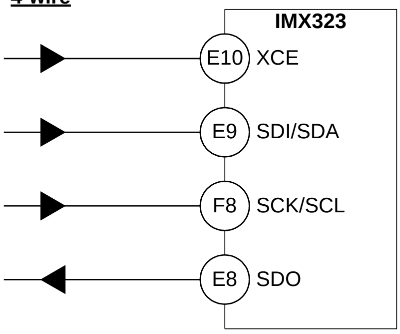


Application circuits shown are typical examples illustrating the operation of the devices.
Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

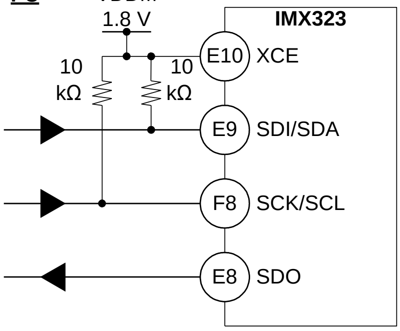
Signal pins

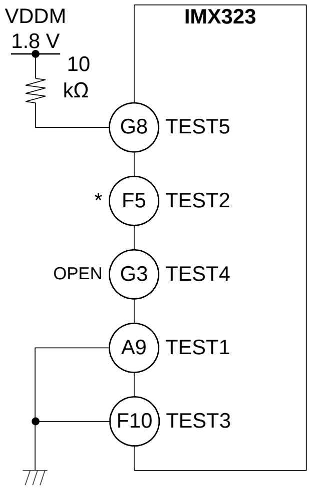


4-wire



I²C

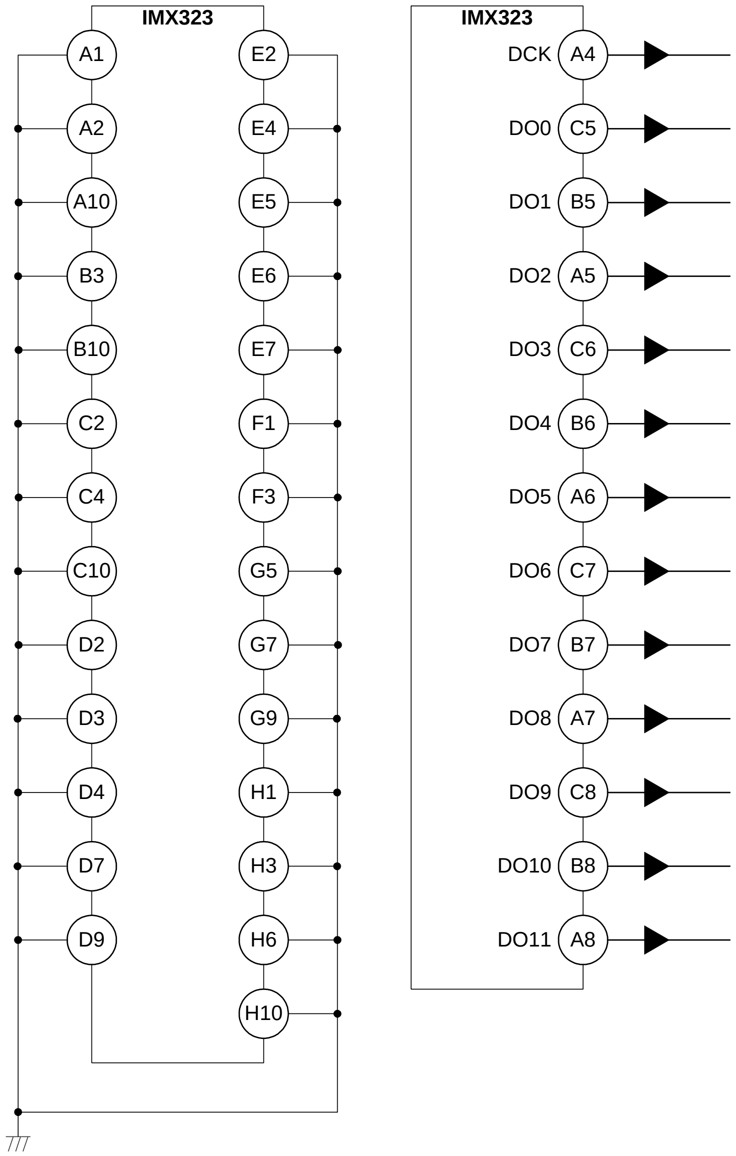




* Normal sync mode: open
DCK sync mode: vertical sync signal

Application circuits shown are typical examples illustrating the operation of the devices.
Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Output pin / GND



Application circuits shown are typical examples illustrating the operation of the devices.
Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

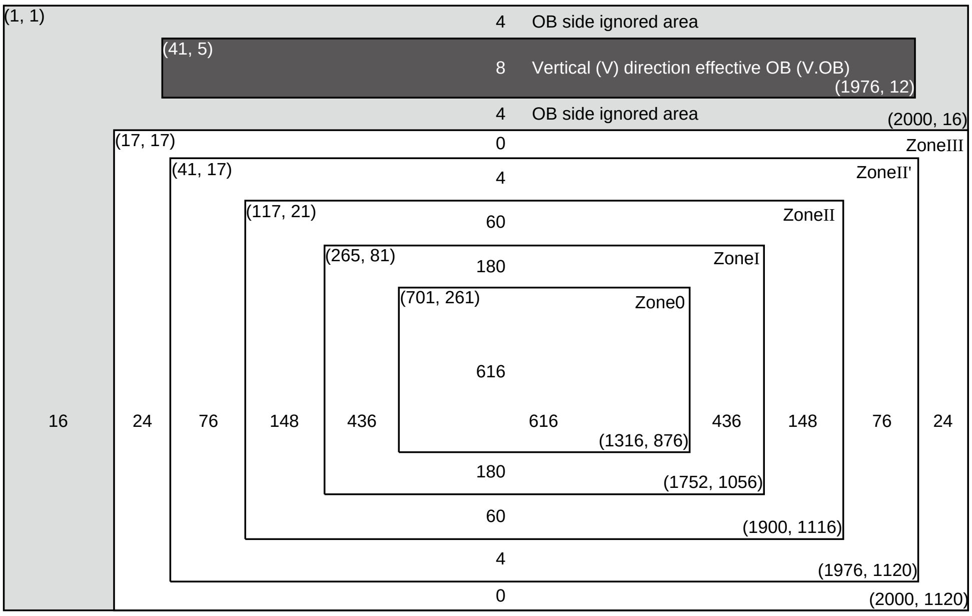
Spot Pixel Specifications

(AV_{DD} = 2.7 V, OV_{DD} = 1.8 V, DV_{DD} = 1.2 V, Tj = 60 ˚C, 30 frame/s, Gain: 0 dB)

Type of distortion	Level	Maximum distorted pixels in each zone				Measurement method	Remarks
		0 to II'	Effective OB	III	Ineffective OB		
Black or white pixels at high light	30 % ≤ D	TBD	No evaluation criteria applied			1	
White pixels in the dark	5.6 mV ≤ D	TBD		No evaluation criteria applied		2	Tj = 60 ˚C 1/30 s integration
Black pixels at signal saturated	D ≤ TBD mV	0	No evaluation criteria applied			3	

Note) 1. Zone is specified based on all-pixel drive mode.
2. D...Spot pixel level.
3. See the Spot Pixel Pattern Specifications for the specifications in which white pixel and black pixel are close.

Zone Definition



Notice on White Pixels Specifications

After delivery inspection of CMOS image sensors, cosmic radiation may distort pixels of CMOS image sensors, and then distorted pixels may cause white point effects in dark signals in picture images. (Such white point effects shall be hereinafter referred to as "White Pixels".) Unfortunately, it is not possible with current scientific technology for CMOS image sensors to prevent such White Pixels. It is recommended that when you use CMOS image sensors, you should consider taking measures against such White Pixels, such as adoption of automatic compensation systems for White Pixels in dark signals and establishment of quality assurance standards.
Unless the Seller's liability for White Pixels is otherwise set forth in an agreement between you and the Seller, Sony Corporation or its distributors (hereinafter collectively referred to as the "Seller") will, at the Seller's expense, replace such CMOS image sensors, in the event the CMOS image sensors delivered by the Seller are found to be to the Seller's satisfaction, to have over the allowable range of White Pixels as set forth as set forth above under the heading "Spot Pixels Specifications", within the period of three months after the delivery date of such CMOS image sensors from the Seller to you; provided that the Seller disclaims and will not assume any liability after if you have incorporated such CMOS image sensors into other products.
Please be aware that Seller disclaims and will not assume any liability for (1) CMOS image sensors fabricated, altered or modified after delivery to you, (2) CMOS image sensors incorporated into other products, (3) CMOS image sensors shipped to a third party in any form whatsoever, or (4) CMOS image sensors delivered to you over three months ago. Except the above mentioned replacement by Seller, neither Sony Corporation nor its distributors will assume any liability for White Pixels. Please resolve any problem or trouble arising from or in connection with White Pixels at your costs and expenses.

[For Your Reference] The Occurrence Rate of White Pixels

The chart below shows the predictable data on the occurrence rates of White Pixels in a single-story building in Tokyo at an altitude of 0 meters. It is recommended that you should consider taking measures against White Pixels, such as adoption of automatic compensation systems appropriate for each occurrence rate of White Pixels.
The data in the chart is based on records of past field tests, and signifies estimated occurrence rates calculated according to structures and electrical properties of each device. Moreover, the data in the chart is for your reference purpose only, and is not to be used as part of any CMOS image sensor specifications.

Example of Occurrence Rates

White Pixel Level (in case of storage time = 1/30 s) (Ta = 60 ℃)	Occurrence Rate per week
5.6 mV or higher	TBD %
10.0 mV or higher	%
24.0 mV or higher	%
50.0 mV or higher	%
72.0 mV or higher	%

Note 1) The above data indicates the average occurrence rate of a single White Pixels that will occur when a CMOS image sensor is left for a week.
For example, in a case of a device that has a 1 % occurrence rate per week at the 5.6 mV or higher effect level, this means that if 1,000 devices are left for a week, a total of 10 devices out of the whole 1,000 devices will have a single White Pixels at the 5.6 mV or higher effect level.

Note 2) The occurrence rate of White Pixels fluctuates depending on the CMOS image sensor storage environment (such as altitude, geomagnetic latitude and building structure), time (solar activity effects) and so on. Moreover, there may be statistic errors. Please take notice and understand that this is an example of test data with experiments that have being conducted over a specific time period and in a specific environment.

Note 3) This data does not guarantee the upper limits of the occurrence rate of White Pixels.

For Your Reference:

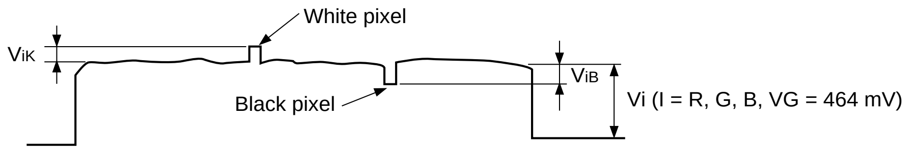
The occurrence rate of White Pixels at an altitude of 3,000 meters is from 5 to 10 times more than that at an altitude of 0 meters because of the density of the cosmic rays. In addition, in high latitude geographical areas such as London and New York, the density of cosmic rays increases due to a difference in the geomagnetic density, so the occurrence rate of White Pixels in such areas approximately doubles when compared with that in Tokyo.

Measurement Method for Spot Pixels

After setting the measurement condition to the standard imaging condition II, and the device drive conditions are within the bias and clock voltage conditions. Configure the drive circuit according to the example and measure.

1. Black or white pixels at high light
   After adjusting the average value of the Gr/Gb signal output to 464 mV, measure the local dip point (black pixel at high light, ViB) and the peak point (white pixel at high light, ViK) in the Gr/Gb/R/B signal output Vi (i = Gr/Gb/R/B), and substitute the values into the following formula.

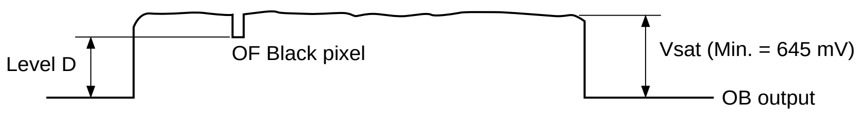
   Spot pixel level D = {(Vi_B or Vi_K)/Vi average value} × 100 [%]



Signal output waveform of R/G/B channel

2. White pixels in the dark
   Set the device to a dark setting and measure the local peak point of the signal output waveform using the average value of the dark signal output as a reference.

3. Black pixels at signal saturated
   Set the device to operate in saturation and measure the local dip point using the OB output as a reference.

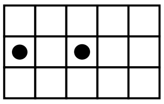
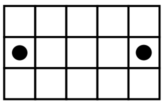
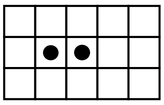
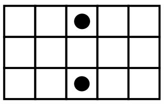
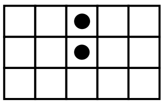


Signal output waveform of R/G/B channel

Spot Pixel Pattern Specifications

Spot pixel patterns are counted as shown below.

List of Spot Pixel Patterns

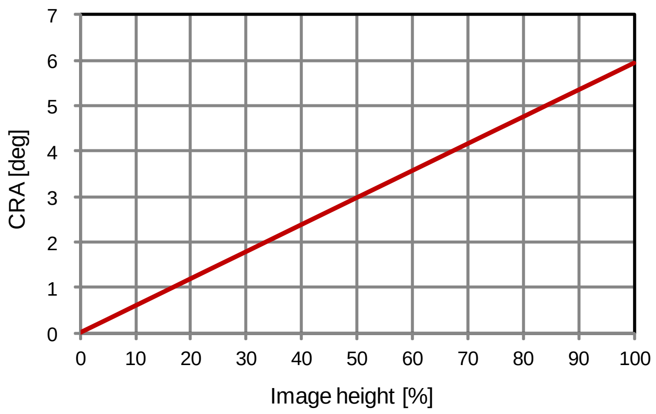
No.	Pattern	White pixel / Black pixel / Bright pixel
1		Rejected
2		Allowed
3		
4		
5		

Note) 1. ●: Black circles indicate the positions of spot pixels. The patterns are specified separately for white pixels, black pixels and bright spots.
(Example: Even when a black pixel and a white pixel are arranged as shown by pattern No. 1, this is not judged as a defect (Allowed).)
2. Sensors exhibiting one or more patterns indicated as “Rejected” are sorted and removed.
3. Sensors exhibiting patterns indicated as “Allowed” are not subject to sorting and removal, and these pixels are instead counted in the number of allowable spot pixels by zone.
4. White pixels and black pixels other than the patterns noted in the table above are all counted in the number of allowable spot pixels by zone.

CRA Characteristics

(Exit pupil distance: -30 mm)

The recommended CRA characteristics is 0.0 degrees all over the image height (0 – 100 %), because the target E.P.D. is infinite.
We assume that the worst case of E.P.D. is -30 mm. The CRA characteristics of -30 mm E.P.D. is described below. The real CRA should be smaller than the table below.



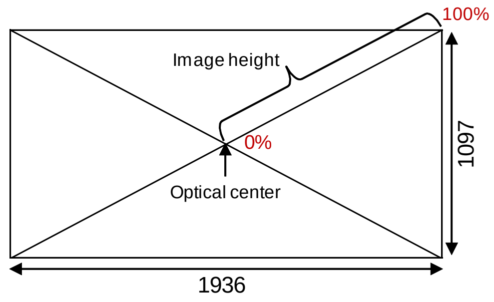


Image height		CRA
(%)	(mm)	(deg)
0	0.00	0.00
5	0.16	0.30
10	0.31	0.59
15	0.47	0.89
20	0.62	1.19
25	0.78	1.49
30	0.93	1.78
35	1.09	2.08
40	1.25	2.38
45	1.40	2.68
50	1.56	2.97
55	1.71	3.27
60	1.87	3.57
65	2.02	3.86
70	2.18	4.16
75	2.34	4.45
80	2.49	4.75
85	2.65	5.04
90	2.80	5.34
95	2.96	5.63
100	3.12	5.93

Notes On Handling

1. Static charge prevention

Image sensors are easily damaged by static discharge. Before handling be sure to take the following protective measures.

(1) Either handle bare handed or use non-chargeable gloves, clothes or material.
Also use conductive shoes.
(2) Use a wrist strap when handling directly.
(3) Install grounded conductive mats on the floor and working table to prevent the generation of static electricity.
(4) Ionized air is recommended for discharge when handling image sensors.
(5) For the shipment of mounted boards, use boxes treated for the prevention of static charges.

2. Protection from dust and dirt

Image sensors are packed and delivered with care taken to protect the element glass surfaces from harmful dust and dirt. Clean glass surfaces with the following operations as required before use.

(1) Perform all lens assembly and other work in a clean environment (class 1000 or less).
(2) Do not touch the glass surface with hand and make any object contact with it.
If dust or other is stuck to a glass surface, blow it off with an air blower.
(For dust stuck through static electricity, ionized air is recommended.)
(3) Clean with a cotton swab with ethyl alcohol if grease stained. Be careful not to scratch the glass.
(4) Keep in a dedicated case to protect from dust and dirt. To prevent dew condensation, preheat or precool when moving to a room with great temperature differences.
(5) When a protective tape is applied before shipping, remove the tape applied for electrostatic protection just before use. Do not reuse the tape.

3. Installing (attaching)

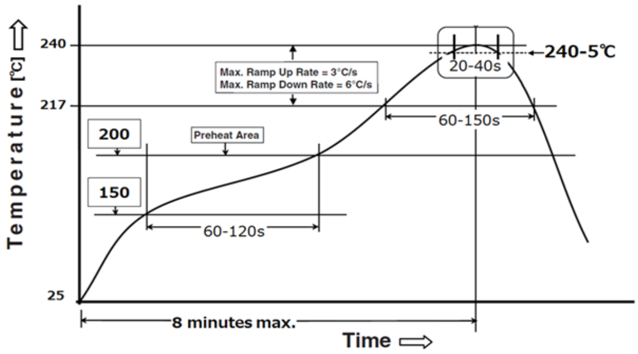
(1) If a load is applied to the entire surface by a hard component, bending stress may be generated and the package may fracture, etc., depending on the flatness of the bottom of the package.
Therefore, for installation, use either an elastic load, such as a spring plate, or an adhesive.
(2) The adhesive may cause the marking on the rear surface to disappear.
(3) If metal, etc., clash or rub against the package surface, the package may chip or fragment and generate dust.
(4) Acrylate anaerobic adhesives are generally used to attach this product. In addition, cyanoacrylate instantaneous adhesives are sometimes used jointly with acrylate anaerobic adhesives to hold the product in place until the adhesive completely hardens. (Reference)
(5) Note that the sensor may be damaged when using ultraviolet ray and infrared laser for mounting it.

4. Recommended reflow soldering conditions

The following items should be observed for reflow soldering.

(1) Temperature profile for reflow soldering (* Conform to J-STD-020E)

Profile Feature	Profile (at part side surface)
Preheat Temperature Min. Temperature Max. Time from 150 to 200°C	 150°C 200°C 60 – 120 seconds
Ramp-up Rate 217 to 240°C	3°C / second max.
Liquidus temperature Time maintained above 217°C	217°C 60 – 150 seconds
Peak package body temperature	240°C
Time within 5°C of the peak temperature	20 – 40 seconds
Ramp-down rate 240 to 217°C	6°C / second max.
Time 25°C to peak temperature	8 minutes max.



(2) Reflow conditions

(a) Make sure the temperature of the upper surface of the seal glass does not exceed 240 °C.
(b) Perform the reflow soldering only one time.
(c) Finish reflow soldering within 72 h after unsealing the degassed packing.
Store the products under the condition of temperature of 30 °C or less and humidity of 60 % RH or less after unsealing the package.
(d) Perform re-baking only one time under the condition at 125 °C for 24 h.

(3) Others

(a) Carry out evaluation for the solder joint reliability in your company.
(b) After the reflow, the DAM area (resin adhesion part) might be discolored.
It is unquestioned except for the remarkable case. (It not affected to reliability.)
(c) Note that X-ray inspection may damage characteristics of the sensor.

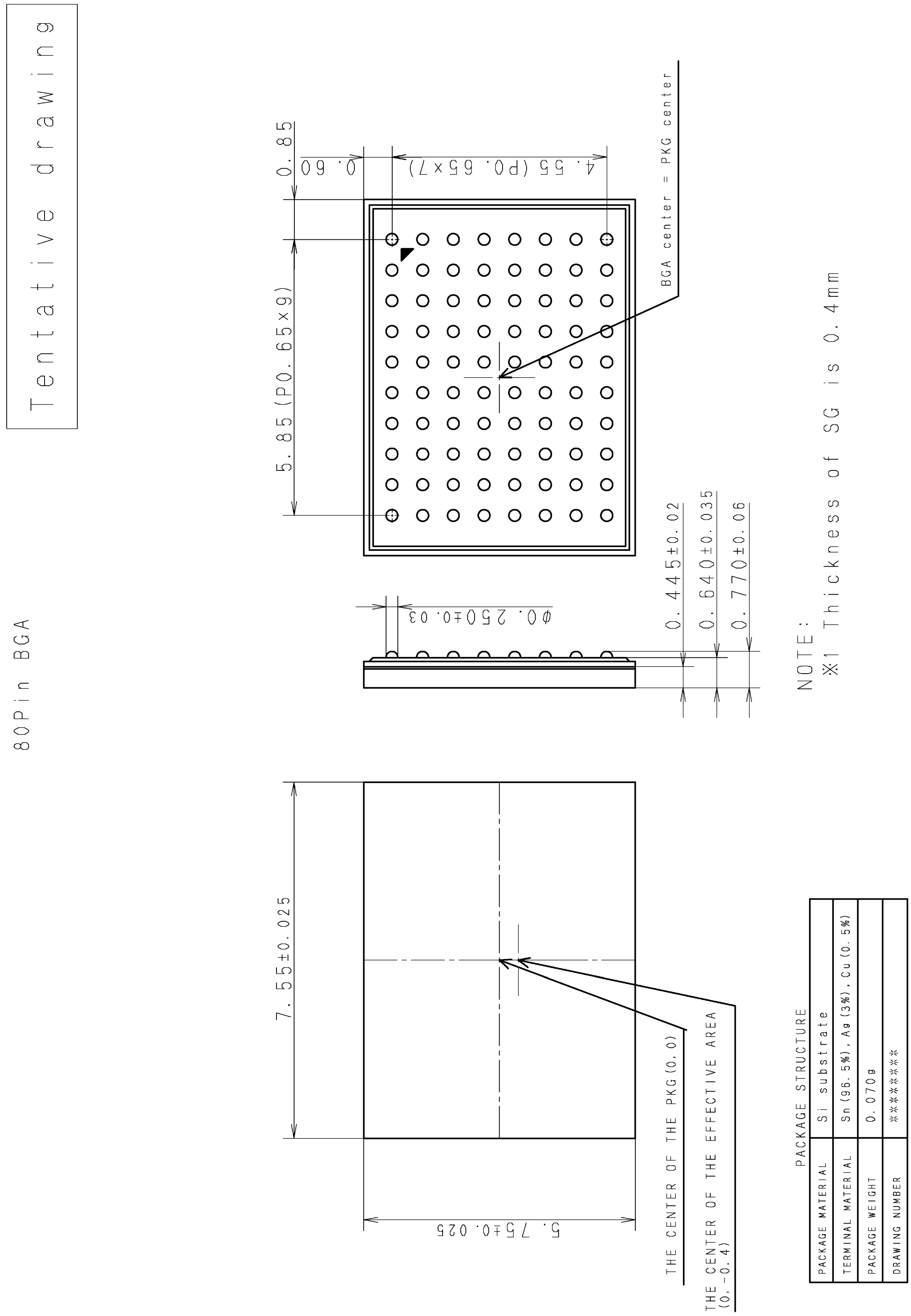
5. Others

(1) Do not expose to strong light (sun rays) for long periods, as the color filters of color devices will be discolored.
(2) Exposure to high temperature or humidity will affect the characteristics. Accordingly avoid storage or use in such conditions.
(3) This product is precision optical parts, so care should be taken not to apply excessive mechanical shocks or force.
(4) Note that imaging characteristics of the sensor may be affected when approaching strong electromagnetic wave or magnetic field during operation.
(5) Note that image may be affected by the light leaked to optical black when using an infrared cut filter that has transparency in near infrared ray area during shooting subjects with high luminance.

Individual-2015.09.18

Package Outline

(Unit: mm)



List of Trademark Logos and Definition Statements

Exmor

* Exmor is a trademark of Sony Corporation. The Exmor is a version of Sony's high performance CMOS image sensor with high-speed processing, low noise and low power dissipation by using column-parallel A/D conversion.